Development of a One-Dimensional Detector for Diffraction Experiments at the Synchrotron Radiation Beam

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Abstract—The work describes a one-dimensional detector for diffraction experiments at a synchrotron radiation beam. The detector is being developed at the Budker Institute of Nuclear Physics, Siberian Branch, Russian Academy of Sciences. Until recently the institute was developing gas one-coordinate detectors, in particular a one-coordinate detector with calculated channels (OD-3M), based on the technology of multiwire proportional chambers. To provide a spatial resolution better than 100 microns at a photon energy in a wide energy range (3-30 keV), it is necessary to use solid-state microstrip or matrix sensors in combination with specialized integrated registration circuits. The developed SOCOD detector, using a microstrip sensor based on gallium arsenide as a registration element, operates in the mode of the direct counting of photons with an energy of more than 3-4 keV and a speed of up to 1 MHz/channel. The work gives a general description of the current version of the detector, a block diagram of the registration channel, the software allowing users to control the operation of the detector and display the results obtained, and the developed algorithm for leveling the trigger thresholds in the channels. The results of electronic tests, the work of the alignment algorithm and their discussion are presented.

Keywords: diffraction experiments, coordinate detectors, photon-counting mode, electronic registration channel, microstrip sensor, specialized integrated circuit, system-on-a-chip, counting-alignment algorithm, registration threshold, counting characteristic

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INTRODUCTION

For more than a quarter of a century, synchrotron radiation (SR) has been used in studies of the dynamics of fast physical and chemical processes. Short radiation beam generated by electron bunches in SR sources make it possible to carry out measurements with high temporal and spatial resolution using coordinate detectors. At the moment, the best results in such experiments are achieved using multichannel coordinate detectors based on semiconductor sensors with strip or matrix structures as sensitive detection elements, where each channel operates either in an integrating or counting mode [1-4].

The counting mode of detector operation is used to study relatively slow processes. In this mode, signals from individual photons are recorded, which, in combination with the potential possibility of selecting photons in terms of energy, opens up the possibility of obtaining more detailed information about the processes under study.

At the Institute of Nuclear Physics, Siberian Branch, Russian Academy of Sciences, detectors for SR experiments have been developed, manufactured, and used on the VEPP-3 and VEPP-4 SR sources for more than two decades [5–15]. In particular, the OD-3M detector, based on the technology of multiwire proportional chambers, has 64 physical channels and 3300 channels calculated on their basis, and a spatial resolution of $\sigma \sim 180 \ \mu m$ at a photon energy of 8 keV. At the moment, two such detectors operate on the SR channels of the Siberian Center for Synchrotron and Terahertz Radiation (SCSR) at the Institute of Nuclear Physics, Siberian Branch, Russian Academy of Sciences [16–18].

At present, the institute is developing a SOCOD single-coordinate X-ray detector operating in the direct photon-counting mode. The detector must pro-



Web-interface

Fig. 1. 96-channel prototype of the SOCOD counting detector: microstrip sensor based on GaAs (a); registration board with microstrip sensor and registration integrated circuit (b); a motherboard that controls the operation of the detector, containing a FPGA running the LINUX operating system with a web-interface (c).

vide a spatial resolution of better than 100 μ m and an angular resolution of about 0.01°, a frame rate of more than 10 kHz, and a speed of up to 1 MHz/channel, which is necessary to achieve a high recording rate of measurement results.

STRUCTURE AND MAIN PARAMETERS OF THE DETECTOR

The layout of the SOCOD counting detector is shown in Fig. 1. The detector consists of a microstrip sensor based on gallium arsenide (GaAs) with a strip pitch of 50 μ m and a strip length of 10 mm (the sensor was provided by the Research and Development Center "Advanced Technologies in Microelectronics" at Tomsk State University). Each sensor strip is connected to an electronic registration channel of a specialized integrated circuit. The registration channels are controlled and data readout is carried out using a field programmable gate array (FPGA). The data is transferred to the user's computer using the processor built into the FPGA.

The structure of the registration channel is shown in Fig. 2. It consists of a 400 mV/fC shaping amplifier, four comparators with controllable thresholds (global and individual), 4–5-bit digital-to-analog converters (DAC) for setting individual thresholds, and 4–8-bit counters that count the number of times the comparators were triggered during a given time interval (frametime). At the end of the frametime, information from the counters is rewritten to the output shift register and then stored in an external memory.

The registration channels have two types of controllable thresholds: global and individual. The global thresholds are set by 6-bit DACs external to the recording integrated circuit. The setting range of the global thresholds is (0-1.5) fC and that of the individual thresholds is (0-0.2) fC. The levels of the global thresholds are fed to the four comparators of each chip and each registration channel is adjusted using the individual thresholds. The global thresholds are used to highlight up to four energy bands in the detected quantum flux. The number of energy bands was chosen based on analysis of the conditions of the planned experiments. The individual thresholds serve to equalize the counting characteristics of the registration channels.

The counting characteristic is the dependence of the counting rate on the comparator threshold for a given value of the input signal. The value of the sum of the individual and global thresholds, at which the count rate is 50% of the maximum value, is equal to the average value of the signal at the input of the comparator, which, in turn, is proportional to the value of the input signal.



Fig. 2. Structure of the detector's registration channel.

To work with the detector, software has been developed that contains a FPGA design and a processor system with a web-interface to control detector operation, displaying the count value in each channel and resources for measuring the counting characteristics. The interface also contains an algorithm for automatically setting individual thresholds to equalize the counting characteristics of the channels, which is fundamentally important for ensuring the uniformity of the detector scale. The task of the algorithm is to set the same threshold values for the largest number of registration channels.

The algorithm consists of three stages: measuring, calculation and correction stages. At the first stage the counting characteristics of the channels are measured and the value of the thresholds corresponding to 50% of the count is calculated. At the second stage, according to the calculation data, a search is carried out for the optimal threshold value, for which the largest number of thresholds found at the first stage, corre-



Fig. 3. Histograms of the distribution of the global threshold values corresponding to 50% of the count rate, before (a) and after (b) the application of the algorithm for the automatic setting of individual thresholds.



Fig. 4. Shape of the signal at the output of the shaping amplifier with an input signal corresponding to 31.1 keV (a) and the dependence of the noise reduced to the input on the capacitance of the signal source at the input (b).

sponding to 50% of the count of individual channels, is in the adjustment range of individual thresholds. At the third stage, by the value of the deviations of these thresholds from the optimal, correction codes are calculated for all channels and are recorded in the DAC of individual thresholds.

The results of the algorithm are shown in Fig. 3. From the histograms of the distribution of the global threshold values corresponding to 50% of the count rate in the channels, it can be seen that approximately 60% of the channels can be made identical.

CURRENT DEVELOPMENT STATUS

To date, the characteristics of the registration electronics of the prototype have been studied in detail. In particular, the conversion coefficients of the amplifiers and the shift of the base levels at the inputs of the comparators were measured. Figure 4a shows the waveform at the output of the shaping amplifier, measured using a broadband digital oscilloscope. The measured signal in magnitude and shape agrees well with the simulation results and corresponds to a formation time of ~300 ns.

The dependence of the noise on the capacitance at the input (Fig. 4b) is approximately three times higher than that according to the simulation results. At the same time, it should be noted that at zero capacitance at the input, the measurement result coincides with the simulation. The reason for the appearance of excess noise is found and is poor filtering of the lowfrequency noise in the reference voltage source. This



Fig. 5. Histograms of the distribution of the gain (a) and baseline offset (b).

shortcoming will be eliminated in the process of chip correction.

The counting characteristics of each channel of the detector with and without a connected sensor were also measured. Based on the obtained characteristics, the channel-transfer coefficients (Fig. 5a) and the baseline offset (Fig. 5b) were determined. It can be seen from the figure that there is a significant spread in the gains and offsets of the baselines of the amplifiers. This spread will be significantly reduced in the process of correcting the specialized integrated-circuit parameters.

CONCLUSIONS

An eight-channel prototype of a specialized integrated circuit for the SOCOD detector designed for SR registration has been developed and manufactured. On its basis, a 96-channel prototype of a singlechannel detector was assembled, and the design of a FPGA and software were developed. Measurements of the main characteristics of the registration channels and electronic tests were carried out. In the future, it is planned to carry out physical measurements of the combined characteristics of the detector (sensor and electronics) on a SR beam under conditions of a real experiment, as well as the design and production of a 64channel full-length integrated circuit.

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CONFLICT OF INTEREST

The authors declare that they have no conflicts of interest.

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