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PHYSICAL FUNDAMENTALS OF MICRO- AND NANOTECHNOLOGIES AND OPTICAL ELECTRONICS

Specialized Integrated Circuit for Coordinate Counting Detectors

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Abstract—A multichannel application specific integrated circuit (ASIC) for registration and processing of signals from microstrip sensors in synchrotron radiation coordinate detectors developed at the BINP SB RAS to equip the SKIF experimental stations is presented. The ASIC contains 64 independent photon registration channels with 4 energy separation thresholds. The range of registered energies is from 3 to 60 keV. The structure and main parameters of the registration channel electronics for direct photon counting are described in detail.

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1. INTRODUCTION

For more than fifty years, synchrotron radiation (SR) has been used in studies of the dynamics of physical and chemical processes [1–4]. Short radiation bursts generated in SR sources with a strictly defined periodicity and short duration (∼1 ns) allow measurements with high spatial and temporal resolutions to be conducted.

These studies record the coordinate distribution of the intensity of radiation passing through the given object, the parameters of which vary due to a physical action or a chemical reaction. These experiments use coordinate X-ray detectors to fix the states of the object at certain time intervals called frames. The length of these frames should be significantly shorter than the characteristic times of the process under study and can vary from tens of minutes for slow processes to tens of nanoseconds for shock-wave processes and detonations.

Currently, the best results in SR-based experiments are achieved using multichannel detectors with a coordinate resolution of $\sim 50\ \mu m$, operating in either counting or integrating modes. In the counting mode, the detectors record responses from each photon that falls in the detector with energies above given values. These detectors are used for relatively slow processes, such as those in small-angle scattering experiments.

Integrating mode detectors are used to study ultrafast processes. A specific feature of these experiments is that high statistical accuracy of measuring the intensity of the flux of quanta passing

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through the sample can be assured by recording in a very short exposure time (frame time) signals out of a large number of signals. Indeed, statistical accuracy of $\sim 0.1{-}0.3\%$ requires $\geq 10^5$ photons to be recorded within a frame of 20–50 ns. This can only be done in the integrating mode of operation of the electronics; unlike the counting mode, the total signal from all photons entering the detector during the frame time is recorded.

The Institute of Nuclear Physics of the Siberian Branch of the Russian Academy of Sciences has developed, manufactured, and used coordinate X-ray detectors for more than 25 years. An example is the OD-3M one-coordinate gas detector [5], which is based on the technology of multi-wire proportional chambers and has a spatial resolution of 180 nm for a photon energy of 8 keV. To ensure a spatial resolution of less than 100 μm in a wide range of photon energies and a speed up to 1 MHz/channel, one should use coordinate microstrip sensors with a strip pitch of 50 μm and an aperture of 50 mm on the basis of silicon or gallium arsenide in combination with multichannel application-specific integrated circuits (ASICs) that provide the necessary parameters in terms of performance, signal-to-noise ratio, and recording speed. It is this that is implemented in the new coordinate X-ray detectors of counting (SciCODE) and integrating types (DIMEX-Si) developed for use at station 1–3 “Fast processes” of the SKIF Center [6–7].

This study aims to develop a 64-channel integrated circuit SciCODE64 for use as a recording electronics element in counting detectors for processing signals from silicon-based microstrip sensors with a stripe pitch of 50 μm.

2. SPECIAL-PURPOSE INTEGRATED CIRCUIT SciCODE64

The ASIC architecture is based on the results of the development and testing of its 8-channel prototype SICOD8A [8]. This development is based on the 180-nm CMOS technology. A 3×5 mm^2 crystal contains 64 identical recording channels, the structure of which is described below.

The structure of the electronic channel SciCODE64 is shown in Fig. 1. The channel consists of an amplifier, four comparators with controlled thresholds, four 8-bit counters that count the number of times the comparators are triggered during a given interval (frame time), four 6-bit digital-to-analog converters (DACs), and two serial I/O registers for setting individual thresholds and reading the content of counters. When the frame time is over, the information from the counters is rewritten into the output shift register and then stored in external memory. The thresholds of comparators are specified using four external voltages (called global thresholds and supplied to the four comparators of all channels) and individual voltages from internal DACs (allowing for individual adjustment of the thresholds of all comparators separately).

The amplifier is the most important part of the recording channel, controlling its main characteristics (the level of its self-noise and speed). The amplifier consists of an input charge-sensitive preamplifier (CSP) and an adjacent shaping amplifier with an adjustable gain factor.

The charge-sensitive preamplifier is an integrating negative feedback amplifier. Its schematic is shown in Fig. 2.

The simplest integrating circuit of the CSP consists of parallel-connected resistance and capacitance, which transmit a negative feedback. The main parameter of the CSP—equivalent noise charge (ENC)—determines the signal-to-noise ratio, which grows with increasing capacitance and declines with increasing resistance of the feedback circuit. The value ENC = 250 ē, corresponding to the signal from a quantum with energy ~1 keV, is achieved at $C_{\rm FB} = 50$ fF and $R_{\rm FB} = 40$ MOhm.

The ability to increase resistance is limited by the average input current generated by both the recorded signals and the leakage current of the signal source, since it leads to a shift in the operating points of transistors. For example, the average input current of the channel with a load of quanta with an energy of 30 keV and an average frequency of 1 MHz (which is limiting for the specified parameters) is 1.2 nA, which at $R_{\rm os} = 40$ MOhm causes a shift of the average potential at the output of the integrating preamplifier of $\approx$50 mV and is significant at a supply voltage of 1.8 V. Figure 3 shows the signals after the CSP and the shaping amplifier.

The influence of the average input current can be significantly weakened by using a so-called active discharge circuit, rather than a passive resistance; the schematic of circuit can be found in [9].

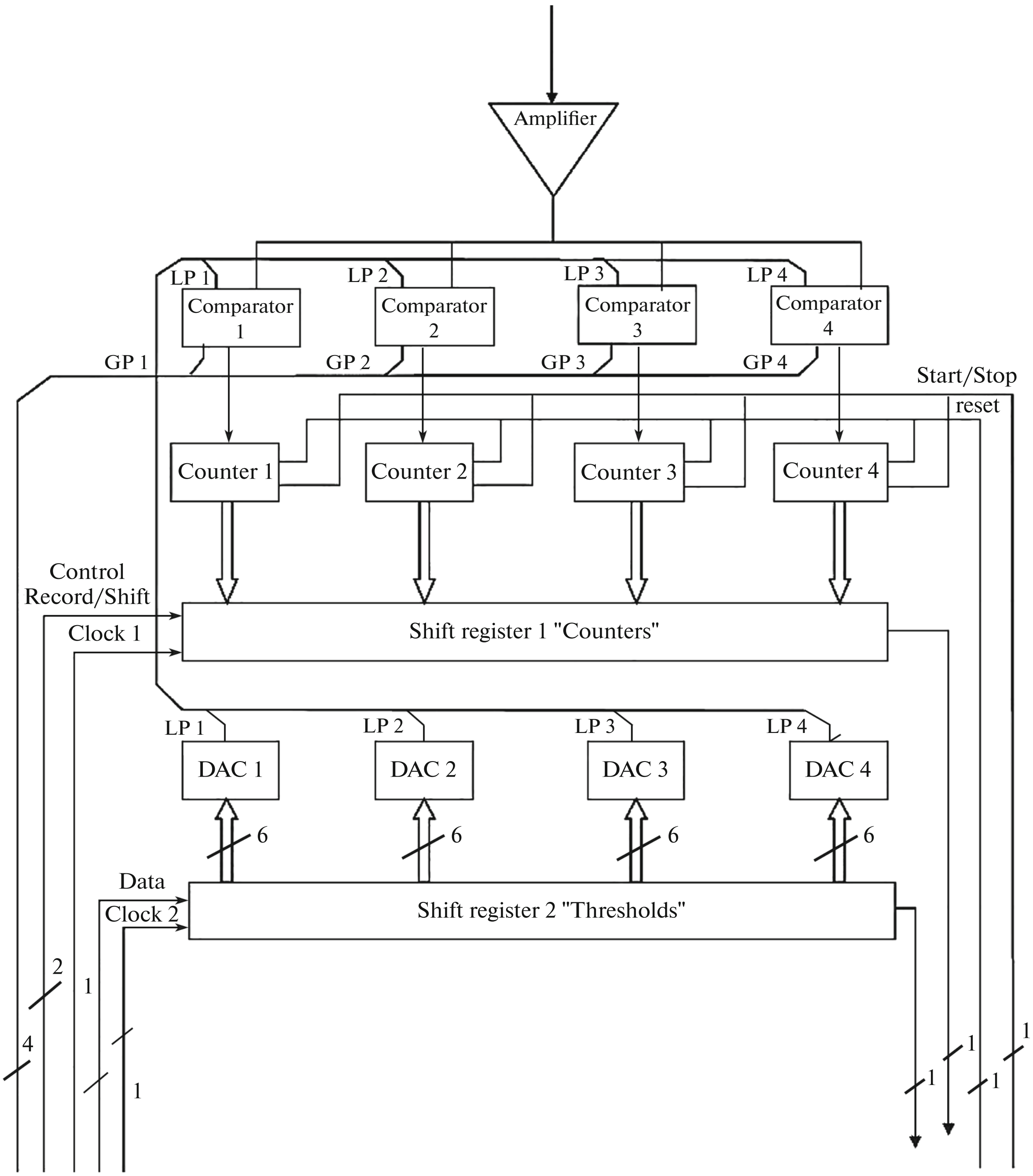

Fig. 1. Electronic registration channel ASIC SciCODE64.

The input signal $U(t)$ for the active discharge circuit is the signal from the output of the CSP. In the simplest case, a current of the form $I(t) = -SU(t)$ is created at the circuit output to be supplied to the integrating capacitor for its discharge. The parameter S has the dimension of conductivity, and its value determines the integration time constant of the CSP:

$$U(t) = \frac{Q(t)}{C_{\text{int}}} e^{-tS/C_{\text{int}}}, \tag{1}$$

where $Q(t)$ is the charge on the integrating capacitance, and $C_{\text{int}}/S = \tau_{\text{int}}$ in terms of an ordinary RC-circuit; $R = 1/S$.

When using sensors with a leakage current comparable to or significantly higher than the average

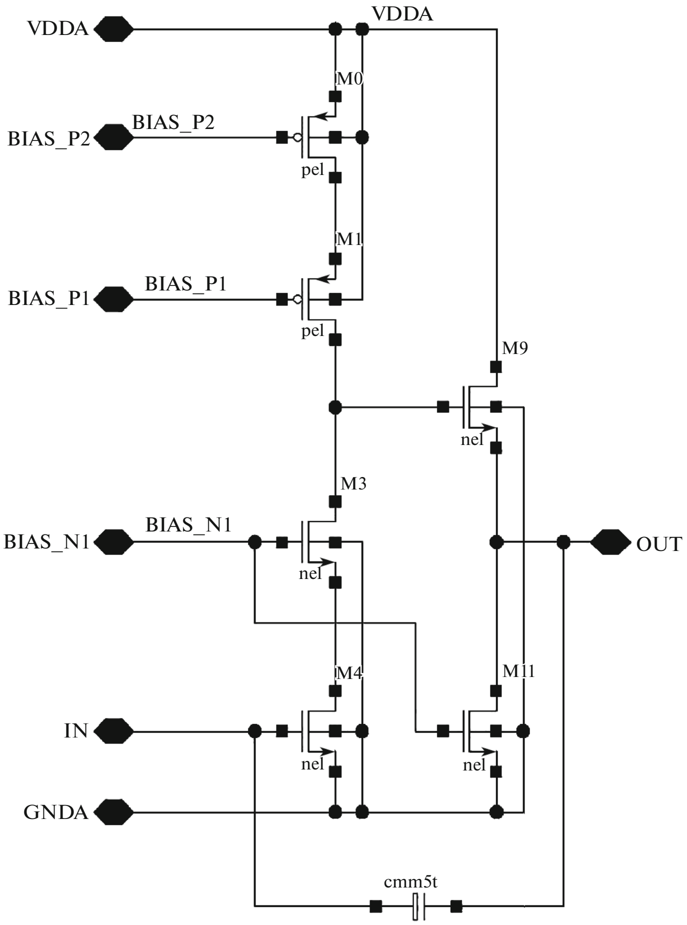

Fig. 2. The charge-sensitive preamplifier circuit.

current from the input signals, one should use a more complex response function of the active discharge circuit:

$$S(t) = S_1 + S_2(1 - e^{-t/\tau_{\text{leak}}}). \tag{2}$$

Here, the parameter S_1 still determines the integration time of the CSP for $t \ll \tau_{\text{leak}}$, and the new parameter S_2 together with τ_{leak} determines the response to change in leakage current. This can occur if the following additional conditions are met:

$$\begin{cases} S_2 \gg S_1, \\ S_1 \gg S_2(1 - e^{-t/\tau_{\text{leak}}}) \quad \text{for} \quad 0 \le t \sim \tau_{\text{int}}. \end{cases} \tag{3}$$

Figure 4 shows the signals at outputs of the preamplifier (A) and the shaping amplifier (B) for $S(t)$ at a leakage current of 30 nA. The transient process in the range from 0 to 10 μs is associated with the fact that the leakage current during the simulation is switched on at time $t = 0$.

An additional important function of the active discharge circuit is the stabilization on potential DC at CSP output, which is necessary for the normal operation of the amplifier stages.

Shaping Amplifier. The formative part of the amplification path (see Fig. 5 for its simplified schematic) consists of two stages. The first stage of the shaping amplifier with a gain factor of ~5 and the second stage with an adjustable gain factor of 1 to 2 are covered by time-dependent negative feedback, which makes it possible to generate a signal at the input of comparators with a length of 300 ns at the base, reducing the total transmission coefficient of amplifiers to unity for times greater than this value. Subsequently, the generated signals are supplied to channel comparators, the thresholds of which are regulated by external voltages.

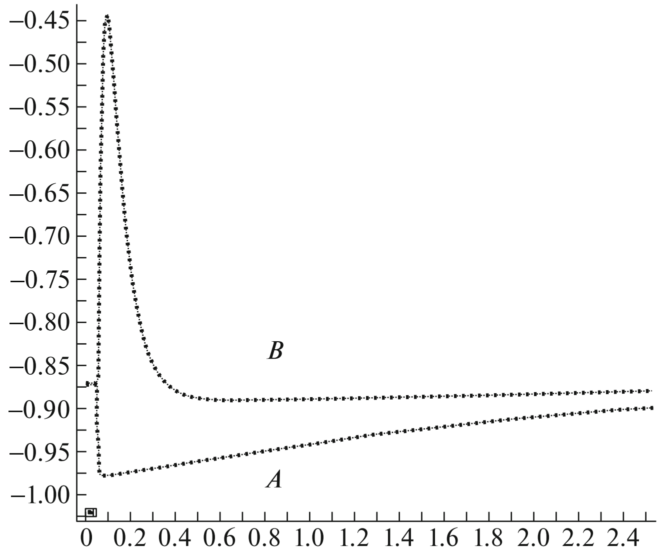

Fig. 3. Signals at the outputs of CSP (A) and shaping amplifier (B).

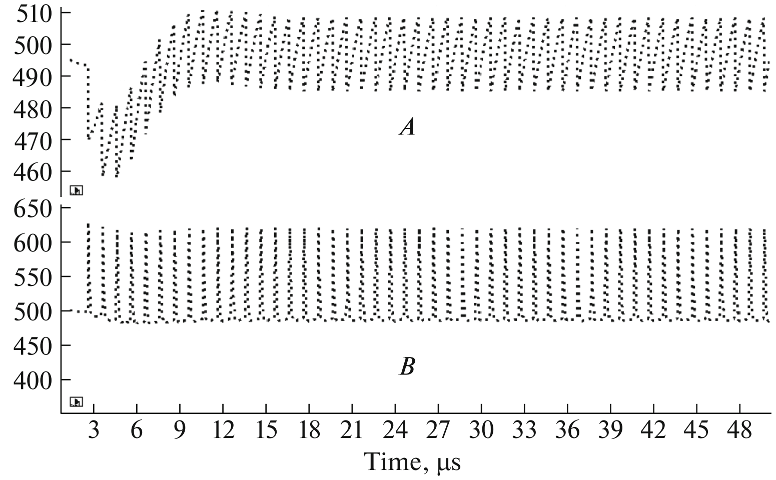

Fig. 4. Output signals of the integrating preamplifier (A) and shaping amplifier (B) at a sensor leakage current of 30 nA.

Digital-to-Analog Converters. Six-bit DACs are built on amplifiers with resistive negative feedback and R-2R matrices with switching keys controlled by the shift register “Thresholds”.

Binary Counters. The eight-bit binary counters used to count the number of comparator operations are built on D-flip-flops with additional keys for transferring data to the output shift register “Counter”.

Managing the Circuit Operation. Comparators use two types of controlled thresholds: global and individual. Four global thresholds are fed to 4 comparators; fine adjustment of the response thresholds of each of them is conducted using individual thresholds. The threshold values of the comparators of each channel are changed using digital-to-analog converters, which add the individual threshold value to the global one.

The shift register “Counter” serves for reading and outputting data from counters. The shift register “Thresholds” contains data for controlling the DAC of individual thresholds, gain factors, turning on/off the supply of a test signal, and the output of the shaping amplifier signal for observation using an oscilloscope.

The shift registers are controlled and the data are read using an external programmable logic integrated circuit.

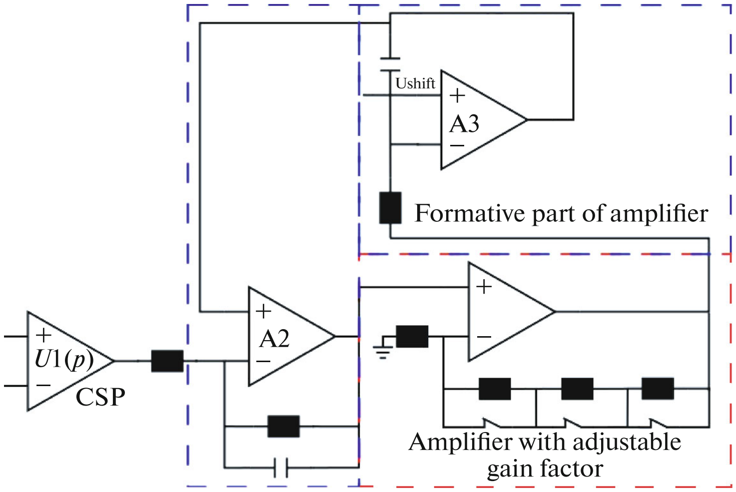

Fig. 5. Formative part of the registration channel.

3. CONCLUSIONS

An integrated 64-channel microcircuit has been developed for reading signals from strips of microstrip coordinate sensors of counting-type X-ray detectors developed at the Institute of Nuclear Physics SB RAS to equip experimental stations at the SKIF synchrotron. The microcircuit is made using the 180-nm CMOS technology on a chip with a size of 3×5 mm^2. Supply voltage of +1.8 V and current consumption of 150 mA are used.

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CONFLICT OF INTEREST

The authors of this work declare that they have no conflicts of interest.

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