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SPIN-RELATED PHENOMENA IN NANOSTRUCTURES

Fabrication and DC/AC Characterization of 3-Terminal Ferromagnet/Silicon Spintronics Devices[1]

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Abstract—CMOS and SOI technology compatible structures and devices are currently intensively investigated by many research groups, since various effects observed in such structures can be relatively easy implemented in electronic devices thereby expanding their functionality. The most promising is the research and development of spintronic devices, which will allow using both electron charge and spin degrees of freedom for transmission, storage and processing of information. In this work we report the fabrication process of 3-terminal (3-T) ferromagnet/silicon devices of two types. First is the planar Fe_3Si/Si 3-T structure with 5 μm gap between closest ferromagnetic electrodes. Second is silicon nanowire back-gate transistor with Fe film source and drain synthesized on SOI substrate. Transport and magnetotransport properties of both devices are investigated.

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1. INTRODUCTION

At present, one of the trends in spintronics is the search for materials and structures for creation of novel devices. The most logical is to build spintronic devices based on silicon because they will be compatible with modern CMOS and SOI technology. Moreover, the lattice inversion symmetry and small atomic number of Si give rise to good spin coherence, enabling its use in spin devices [1]. The room-temperature spin operation in Si has been a significant milestone in Si spintronics. One of the ways to achieve it is through electrical spin injection into Si, which has been intensively studied [2]. Good candidate for application as ferromagnetic (FM) injector is iron silicide Fe_3Si, since it has a Curie temperature of about 800 K, spin polarization of 45% [3] and can be epitaxially grown on semiconductor (SC) substrates [2]. Nevertheless to achieve efficient spin injection in SCs it is necessary to solve a number of problems, like: synthesis of the structure with smooth interface between SC and FM, reduction of defects and localized states concentration at the interface [4], eliminating the conductivity mismatch problem [5]. The search for the optimum device topology and the way to manipulate spin transport is still underway. It is clear that the main difficulties, one way or another, are related to the synthesis of structures and devices. Therefore, in this paper we present a new fabrication process of the 3-terminal (3-T) ferromagnet/silicon devices. Observed transport and magnetotransport properties of devices shows that our technology is yet another promising approach to developing spintronic devices of new type.

2. EXPERIMENTAL

The Fe_3Si film was epitaxially grown on boron-doped silicon substrate *p*-Si(111) (with resistivity of 7.5 Ohm cm) at 400 K by molecular beam epitaxy (MBE) under ultra-high vacuum conditions (UHV) in Angara chamber [6]. Characterization confirmed single crystallinity of film was done by reflective high-energy electron diffraction, X-ray diffraction, and scanning and transmission electron microscopy (SEM and TEM) [7]. The Fe polycristalline film was deposited on the boron-doped silicon (100) on insulator (SOI) wafer (with resistivity of 18 Ohm cm) by thermal evaporation under UHV in the same chamber. As shown in Fig. 1 the final structure consists of handle Si, buried oxide (BOX) layer with thickness 200 nm, 100 nm silicon on insulator and 14 nm iron film.

To synthesize 3-T ferromagnet/silicon devices based on Fe_3Si/Si and Fe/SOI structures different techniques were used. Conventional photolithography process and wet chemical etching were utilized for Fe_3Si/Si. More complicated process was applied to Fe/SOI structure including e-beam lithography, wet and anisotropic reactive ion etching. Our processing methods were examined through characterization of

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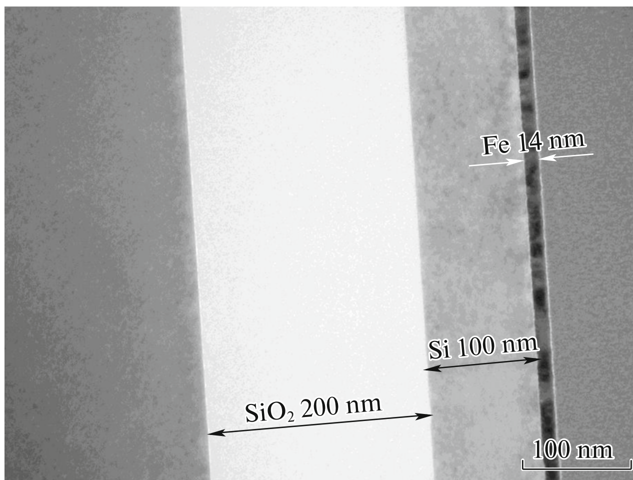

Fig. 1. TEM image of Fe film deposed on SOI wafer.

final device by SEM, TEM, atomic force microscopy (AFM) and magneto-optical Kerr effect (MOKE) microscopy with the help of NanoMOKE 2 installation. Transport and magnetotransport properties measurements of the devices were performed using Keithley 2634b SourceMeter and Agilent E4980A LCR-meter. Investigations of dc/ac charge carrier transport were carried out in cryogenic probe station Lakeshore EMPX-HF 2 and homebuilt facility, which included a helium cryostat and electromagnet. The temperature ranged from 4.2 to 300 K and magnetic field swept up to 1 T.

3. RESULTS AND DISCUSSION

3.1. 3-T Device Processing

At first before etching Fe_3Si film was coated by mask using the standard photolithography method. Film area coated with photoresist was protected from etching (acid) solution while the rest of the film was removed in a solution of hydrofluoric acid and nitric acid $HF:HNO_3:H_2O = 1:2:400$. Surface treatment was carried out in the etching solution with constant agitation and temperature of 22°C followed by cleaning in distilled water. Etching rate for Fe_3Si alloy film was 52 Å/s. To control the etching process a vertical etching profile and roughness of the boundary were measured by AFM after the film removal process. Analysis of AFM data provides an estimate that angles of the side walls do not exceed 3 degrees. We can concluded that etching occurred vertically, yielding high quality structures. Complementary verification of successful etching was probed by MOKE microscopy. This technique is useful to determine whether a ferromagnetic material is left on the substrate after the etching. Using this method we verified that the Fe_3Si film was completely etched away in the areas unprotected by photoresist mask and that the electrodes were, indeed, ferromagnetic. Schematic of the Fe_3Si/Si 3-T planar device is shown in Fig. 2a. Distance between FM injectors is 5 μm.

Schematically depicted in Fig. 2a is the silicon nanowire back-gate transistor with Fe injector electrodes, which was fabricated as follows. Fe/SOI structure was covered by AZ 2035 nL of resist with the thickness 300 nm and then exposed by e-beam lithography (Raith VOYAGER) in accordance with the template containing negative images of dumbbell. The bar between edges of the dumbbell formed the silicon nanowire. The width of nanowire varied from 300 nm to 3 μm. After resist e-beam exposure the Fe film was etched in aqueous solution of nitric acid. At this step we slightly overexposed sample to the isotropic wet etchant to achieve dissolving of the Fe thin bar under the protective mask by one micrometer undercut. This over etching technique allowed us to remove the iron from the top of the nanowire while keeping the same photoresist mask for the second self-aligned plasma etching step. Next, silicon was removed by CF_4 reactive plasma and then the resist was stripped. Thus fabricated silicon nanowire on silica has FM electrodes on its edges, which was confirmed by AFM and SEM.

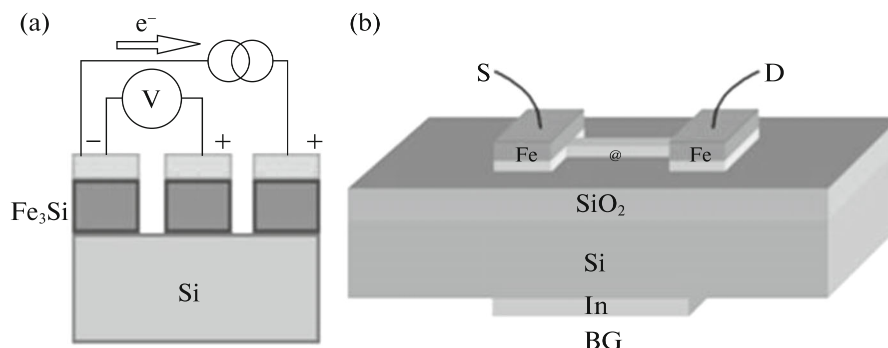

Fig. 2. Schematic of the 3-T devices: (a) planar Fe_3Si/Si structure, (b) silicon nanowire back-gate transistor with Fe injector electrodes.

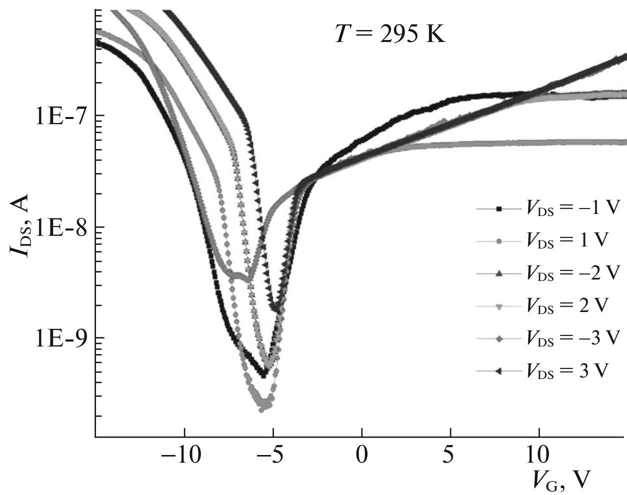

Fig. 3. Typical drain current I_{DS} versus drain voltage V_G curves for silicon nanowire back-gate transistor at different drain voltage V_{DS}.

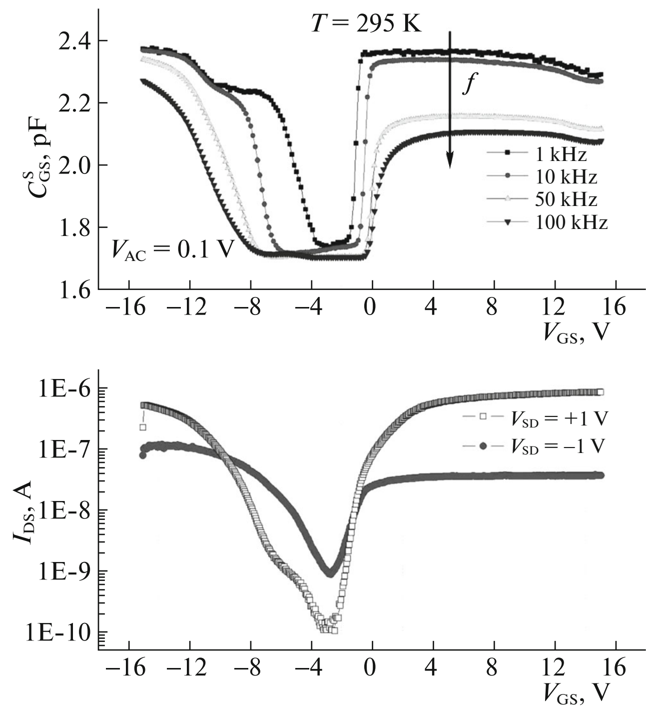

Fig. 4. Typical curves of the gate-source capacitance C_{GS} and drain current I_{DS} versus back-gate voltage V_{GS} of silicon nanowire transistor. *CV*-curves are measured at different frequencies and IV- at different V_{SD} voltages.

Finally, in order to provide the control of charge/current and electrostatic potential in the device channel we placed indium ohmic contact on the substrate back side. This contact served as transistor back-gate.

3.2. Transport Properties

In the Fe_3Si/Si 3-T planar device spin accumulation effect was found by Hanle method [8]. Magnetic field dependences of electrical voltage measured in perpendicular magnetic field geometry (Fig. 2a) has Lorentzian shape which provides supporting evidence for the electrical spin injection from FM Fe_3Si contact to silicon wafer inferring the electrons' spin precession [8, 9]. We believe that spin-dependent transport between Fe_3Si and *p*-Si is realized by tunneling through the Schottky barrier. By measuring the *I*–*V* characteristics of fabricated Fe_3Si/Si Schottky diode we estimated the barrier height to be 0.57 eV. Such value can provide necessary conditions for spin injection from Fe_3Si to *p*-Si.

For the Fe/SOI back-gate nanowire transistor we carried out the transport measurements. Transfer characteristics demonstrate behavior of pseudo MOSFET or nanowire FET with Schottky source/drain contacts (Fig. 3). Similar results had been reported elsewhere [10]. By taking derivative of IV-curves we estimated device maximum transconductance 0.256 mS/mm. Device CV-characterization results are shown in Fig. 4. The gate-source capacitance C_{GS} versus gate voltage reveals MOS capacitor behavior. There is sudden drop of capacitance at small negative gate bias followed by gradual recovery at more negative voltages. This recovery is slower at higher frequency measurements. We attribute the abrupt C_{GS} change to inversion layer and the gradual C_{GS} change to accumulation layer formation in the device channel. Results of IV-curves measurements also shown in Fig. 4 validate out guess.

So far we haven't found in-plane magnetic field influence on the charge transport in our Fe/SOI devices. Further research effort using different transistor geometry and FM injector contacts and barrier shapes is underway.

4. CONCLUSIONS

Two types of 3-T ferromagnet/silicon devices were synthesized using different approaches combining photolithography, e-beam lithography, wet and plasma etching. First is the planar Fe_3Si/Si 3-T structure with 5 μm gap between closest ferromagnetic electrodes. In this structure spin accumulation effect was found. Another 3-T fabricated device is silicon nanowire back-gate transistor with Fe injector electrodes. The width of nanowire varied from 300 nm to 3 μm. Transfer characteristics of transistor demonstrate behavior of pseudo MOSFET or nanowire FET with Schottky source/drain contacts. We attribute the observed transport peculiarities to consecutive formation of inversion layer and accumulation layer in the device channel at voltage sweeping. We believe that

our technology is yet another promising approach to developing spintronic devices of new type.

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