Synthesis and transport properties of FET based on Heusler alloy thin films formed by rapid thermal annealing

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A V Lukyanenko[1,2], A S Tarasov[1,2], L V Shanidze[1,2], I A Yakovlev[1], F V Zelenov[1], A N Masugin[3], A B Ivanov[1], F A Baron[1] and N V Volkov[1]
[1] Kirensky Institute of Physics, Federal Research Center KSC SB RAS, Krasnoyarsk 660036, Russia
[2] Institute of Engineering Physics and Radio Electronics, Siberian Federal University, Krasnoyarsk 660041, Russia
[3] Reshetnev Siberian State University of Science and Technology, Krasnoyarsk 660037, Russia

Abstract. In this work we show a preparation technique of Co_2FeSi full-Heusler alloy thin films on silicon-on-insulator (SOI) substrates, employing rapid thermal annealing (RTA). The films of the Co_2FeSi alloy were formed by a silicidation reaction, caused by RTA, between the ultrathin SOI (001) layer and the Fe/Co layers deposited on it. It is assumed that this technology is compatible with the process of formation of a half-metal source-drain in an advanced CMOS and SOI technology and will be applicable for the manufacture of a source-drain of a field-effect transistor. Schottky barrier field-effect transistors (FET) with a back-gate, based on silicon nanowires with source and drain of a Co_2FeSi film, synthesized on an SOI substrate, were manufactured. The transport properties of the device were investigated.

1. Introduction

Silicon nanowires (SiNW) and devices based on it continue to attract researchers for a long time. The properties of NW allow creating a variety of devices on its basis for a wide range of applications. The use of NW as components for future nanoelectronic devices seems very attractive from the point of view of the possibility of integration into the modern silicon technology. Silicon nanowires (FET NW) field-effect transistors are increasingly used not only in the basic research of physical processes in small sizes, but also as highly sensitive sensors for detecting a wide range of molecules. Today MOS-based sensors are widely distributed as commercial ones. But considered in this work, FET-type sensors have more advantages compared to traditional ones, due to their reduced shape, size and lower price.
For the formation of nanoscale wire current channel, there are two main approaches "bottom-up" and "top-down." The bottom-up approach implies the use of self-assembly processes. Among a number of experimental studies [1, 2], devices based on silicon nanowires were fabricated using a bottom-up approach, which often encounters difficulties in controlling the doping process and the formation of contacts. But the manufacture of NW on site, without the need for their transposition is possible with the use of modern infrastructure of silicon production. Devices based on SiNW, made using the top-down approach, show better control and reproducibility in these parameters. And within the framework of simple integration, as well as the possibility of subsequent implementation, the most promising is the use of a top-down approach, using existing silicon technologies.

At the moment, the focus is on traditional structures of the field-effect transistor with *n-p-n*-doping, which requires complex technological stages of doping [3, 4]. As part of this work, we will demonstrate that nanowires with Schottky contacts can be used as field effect transistors. They are of great interest as an alternative to traditional structures with doped source and drain. This approach avoids the need for doping by replacing source / drain [7] transitions with metal / semiconductor transitions, leaving the nanowire undopped [8]. Field-effect transistors with a Schottky barrier have a number of advantages, including simple and affordable manufacturing technology, as well as bypassing complex manufacturing problems, such as precise control of the type and level of doping, as well as the formation of reliable ohmic contacts.
The use of spin degrees of freedom for the transfer, storage and processing of information will allow to make another qualitative leap in electronics. The open question is the creation of the active element of spin electronics. From the point of view of technology and integration, it would be attractive to use FET geometry for the implementation of a spin transistor. Ferromagnetic metal should provide high spin polarization of conduction electrons. It is technologically most convenient to use 3d metals and their alloys. Iron silicides or Heusler alloys containing Si are good candidates to be used as a FM injector [5]. One of the advantages is the possibility of the formation of the drain and source of the field-effect transistor using a controlled silicidation process, induced by rapid thermal annealing (RTA). When using silicide, abrupt metal / nanowire transitions can be achieved. Consequently, local changes in the contact area as well as in geometry are avoided. For charge transfer this means that two energy barriers are introduced in the current path. The thickness of these barriers is effectively controlled by the gate due to the enhancement of the electric field in the area of the end metal electrode. The on state for a sufficiently small gate length is specified by tunneling through the Schottky barriers, while the off state is controlled by thermionic emission through a high and thick energy barrier. The possibility of the formation of silicon nanowires in the downstream process from top to bottom using bulk silicon substrates or silicon on an insulator gives this technology the possibility of full integration into integrated electronic systems.
SiNW FET for spintronic devices will be very sensitive to the quality of the interfaces between the drain / source and nanowires. A necessary condition for the presence of ferromagnetic elements leads to a number of restrictions. Using the top-down process of forming the current channel, in combination with the RTA process of forming the drain / source of FET, provide the necessary quality and ease of manufacture of devices. The method of forming drain / source contacts from Heusler Co_2FeSi alloys on silicon-on-insulator-type substrates using RTA will bypass the problem of introducing ferromagnetic elements into semiconductor technology and the quality problems of interfaces between ferromagnetic and semiconductor elements.

2. Experimental

Nanowire (NW) devices are formed on commercially available boron doped silicon on insulator (Simox SOI) substrates (with resistivity of 18 Ω cm) using Raith VOYAGER e-beam writer. The formation of the conductive channel and contact pads was carried out from the upper (device) silicon layer, using the common AZ 2035 nLof resist at different exposure doses for current channels and areas of the contact pads of Figure 1 (a). Then, to achieve the desired silicon topology, a dry chemical reactive-ion etching (RIE) stage followed. The etching of silicon over the entire depth (Si - 100 nm) to the dielectric layer (SiO_2 - 200 nm) occurred pulsed for 10 seconds in the plasma of a CF_4 gas. To thin the silicon layer, preliminary thermal annealing was performed at a temperature of 1000-1100 ºC in an atmosphere of dry O_2 at atmospheric pressure, to form SiO_2. The stage of optical lithography is necessary for the formation of windows on the contact pads (drain / source) before the Co and Fe deposition process. Previously, an etching of a SiO_2 film in an HF solution in the area of contact pads was performed. Then, in one technological cycle, Co and Fe films (45 nm and 24 nm, respectively) were deposited by electron beam sputtering (EBS) according to the choice of the stoichiometric

composition of the compound in Figure 1 (b). After the lift-off lithography, the substrate was thoroughly cleaned of residual resistive mask. Co_2FeSi alloy films are formed by a silicidation reaction induced by rapid thermal annealing (RTA) between the ultra-thin Si (001) layer and the Fe / Co layers deposited on it. The RTA process was carried out at 700-800 ºC in N_2 atmosphere for 4 minutes to form Co_2FeSi Figure 1 (c). The layer of buried SiO_2 oxide SOI substrate prevents the diffusion of metals into the substrate during the silicidation process [9]. As a result, the devices represent itself silicon nanowires with half-metal drain and source (Figure 1 - (c)). A series of devices with a current channel width from 300 nm to 3000 nm was manufactured. A typical atomic force microscope (AFM) image of the NW current channel of 500 nm is shown on inset to Figure 1. AFM data exhibit good NW smoothness and the verticality of the side walls of the current channel. To create the back gate of the field-effect transistor, an ohmic contact of indium was formed on the back side of the SOI substrate.

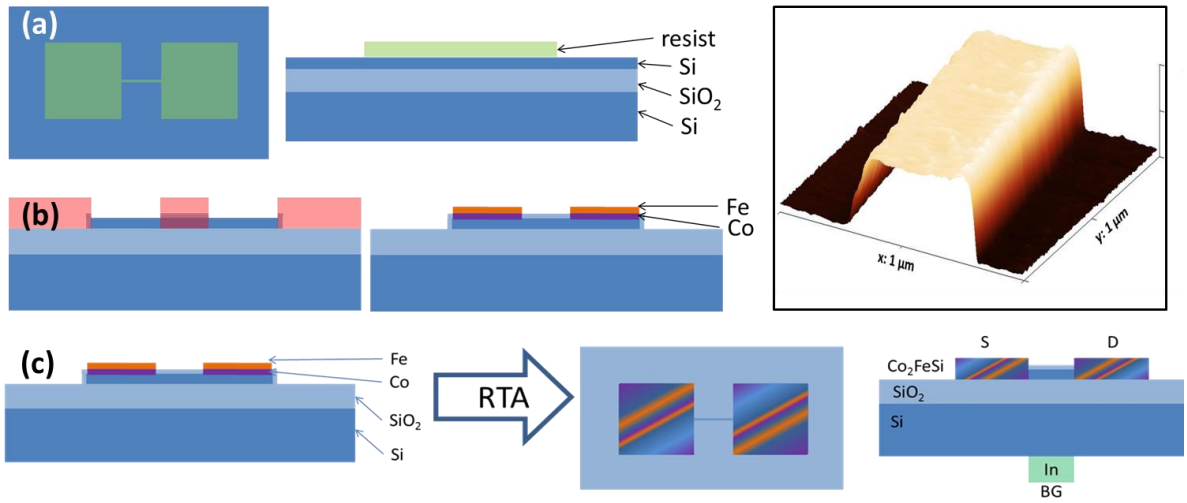

Figure 1(a, b, c) The main technological stages of the formation of devices (a) - (c). Inset: AFM image of a 500 nm wide device.

3. Results and discussion

The devices obtained measured the transport properties in EMPX-HF probe station (LakeShore cryotronics). For Co_2FeSi /SOI back-gate nanowire transistor transport properties were studied. Transfer characteristics demonstrate behavior like pseudo MOSFET or nanowire FET (NWFET) with Schottky source / drain contacts. The transport measurements of the device obtained, as can be seen from Figure 2, demonstrate the typical behavior of an NWFETs. In the accumulation mode, the Drain current between on-state and off-state differs by about 4 orders of magnitude for all devices.
The devices show ambipolar characteristics with both *p*- and *n*-type conductions depending on the gate bias. However, at a gate voltage of 13V, the drain current in the inversion mode is approximately 3 orders of magnitude less than the drainage current in the accumulation mode. This is clearly seen in Figure 2(b), where presented drain current versus drain voltage characteristics.
In addition, from Figure 2(a) it can be seen that the conductivity of the nanowire is not monotonously dependent on its width. The maximum drain current is observed for a device with a 700 nm wide nanowire. This result was unexpected for us and requires additional research beyond the scope of this article.

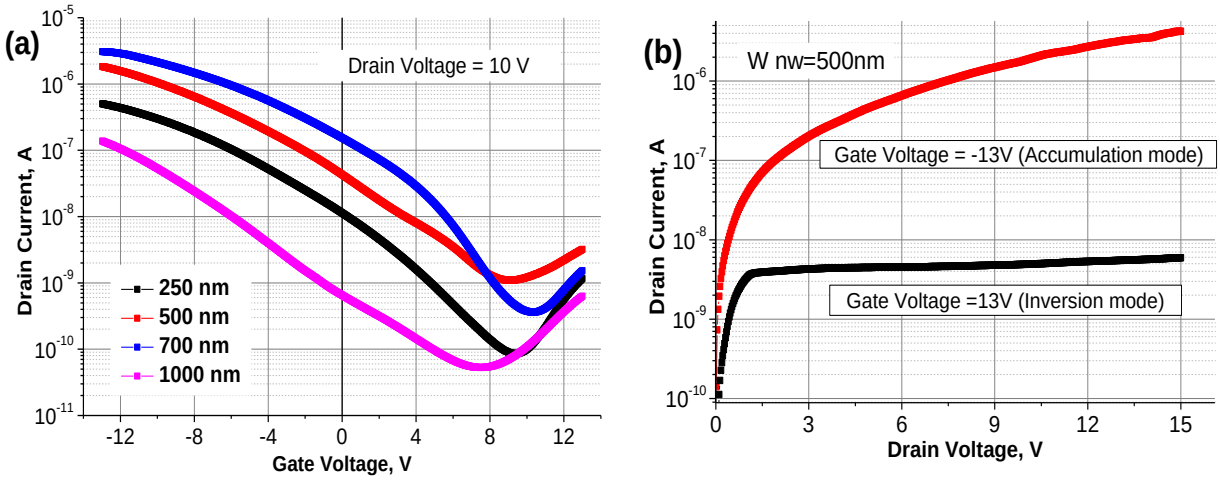

Figure 2(a, b). (a) The transfer characteristics Co_2FeSi/SOI back-gate nanowire transistor with a channel width of width of 250 nm to 1000 nm plotted on a semilog scale at different voltages on source-drain; **(b)** Output characteristics device in inversion and accumulation mode with a channel width of 500 nm.

The use of geometry with a back gate leaves the current channel open and allows the use of NWFET as a highly sensitive electrical sensor. The main sensitive mechanism of a simple sensor based on NWFET, includes the adsorption and isolation of molecules on the surface of the nanowire, which affects the electrical characteristics of the transistor [10].
The use of a top-down process of current channel formation combined with the RTA process of formation of a source/drain of a transistor provides the necessary quality and simplicity of device creation.

Acknowledgments
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