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Technique for Fabricating Ferromagnetic/Silicon Active Devices and Their Transport Properties

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Abstract—Semiconductor nanowires are unique materials for studying nanoscale phenomena; the possibility of forming silicon nanowires on bulk silicon-on-insulator substrates in a top-down process ensures complete incorporation of this technology into integrated electronic systems. In addition, the use of ferromagnetic contacts in combination with the high quality of ferromagnetic–semiconductor interfaces open up prospects for the use of such structures in spintronics devices, in particular, spin transistors. A simple approach is proposed to create semiconductor nanowire-based active devices, specifically, bottom-gate Schottky-barrier field-effect transistors with a metal (Fe) source and drain synthesized on a silicon-on-insulator substrate and the transport characteristics of the designed transistors are investigated.

Keywords: silicon on insulator, transistor, Schottky barrier, electron lithography, nanowire, reactive ion etching, electron transport

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INTRODUCTION

Silicon nanowire-based field-effect transistors are increasingly used both in fundamental investigations of physical processes and as high-sensitivity sensors for detecting a wide range of molecules. Metal–oxide–semiconductor (MOS) sensors are the most widely used commercially; however, the field-effect transistor-type sensors discussed here have more advantages over conventional sensors, since they are small and inexpensive. Silicon nanowires exhibit unique characteristics, including a small diameter and quasi-one-dimensional current transport [1]. In addition, the high surface area-to-volume ratio typical of nanowires makes their electronic properties sensitive to surface and near-surface charge. Therefore, nanowires have a high potential of application ranging from gas sensors to nanobioelectronic devices [2, 3].

A nanowire current channel can be formed in two ways: bottom-up or top-down. The bottom-up approach implies self-assembly [4]. In experimental works [5, 6], silicon nanowire-based devices were formed bottom-up. In this approach, it is often difficult to control the processes of doping and forming contacts, while the parameters of silicon nanowire-based devices fabricated using the top-down approach are easier to control and exhibit better reproducibility. The top-down approach seems more promising for easy integration and subsequent implementation using available silicon technologies.

At present, attention is focused on conventional field-effect transistor structures with *n–p–n* doping, which requires complex technological stages to be involved [7, 8]. Schottky-barrier field-effect transistors have some advantages; in particular, they are easy to manufacture, can be fabricated at low temperatures, and do not require doping and subsequent activation stages [9]. This approach to the device geometry makes it possible to replace source–drain junctions with metal–semiconductor junctions, while the nanowire stays undoped [10]. These features are highly desirable for nanowire devices, since they exclude complex production problems, e.g., precise control of the doping type and level and formation of reliable ohmic contacts.

The geometry of a bottom-gate nanowire transistor is well-suited for use as a high-sensitivity sensor, since the current channel remains open for the chemical probing of a wide range of compounds. In this study, it is shown that the Schottky-contact nanowires can be used as field-effect transistors and high-sensitivity electric-field sensors or give grounds for designing a spin transistor. The possibility of forming silicon nanowires in a top-down process with bulk silicon-on-

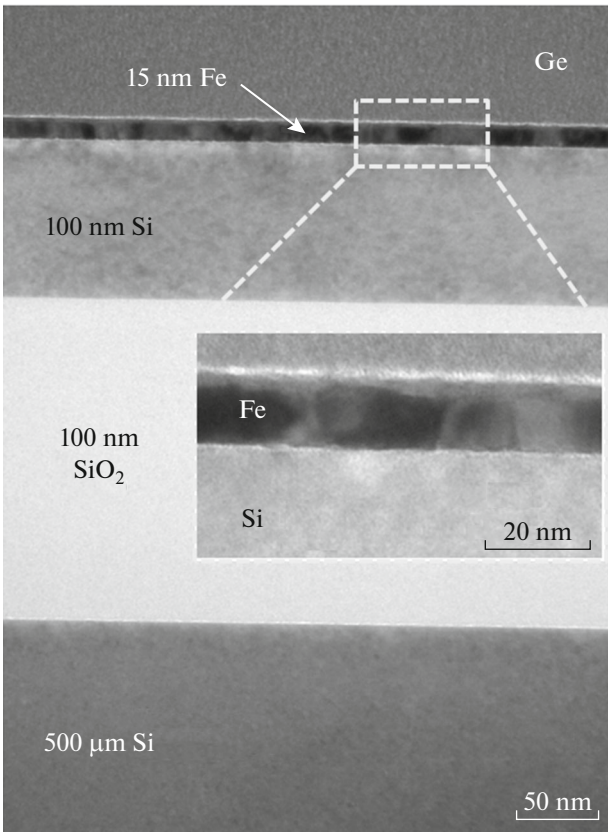

Fig. 1. Cross-sectional TEM image of the Fe/SOI structure with the layer materials and thicknesses indicated.

insulator (SOI) substrates enables full integration into electronic systems [11].

EXPERIMENTAL

To precede the lithography stage, an Fe film was grown on a SOI substrate by thermal evaporation in ultrahigh vacuum. During synthesis, commercial SIMOX SOI boron-doped wafers with a resistivity of 18 Ω cm (doping of 10^{15} cm^{-3}), a Si(100) device-layer thickness of 100 nm, and a buried-oxide-layer thickness of 200 nm were used. Before loading into the growth chamber, the substrates were chemically cleaned using the technique described in [12]. Before iron deposition, the native oxide was removed from the silicon wafer surface by annealing in an ultrahigh vacuum (a residual pressure of 10^{-8} Pa) at a temperature of 400°C for 30 min. Figure 1 shows cross-sectional transmission electron microscopy (TEM) images of the synthesized structure obtained on a Hitachi HT-7700 microscope. The structure consists of a 15-nm-thick Fe layer, 100-nm-thick Si layer, 200-nm-thick SiO_2 layer, and 500-μm-thick Si layer. It can be seen that the Fe film is formed by coarse crystallites 20–30 nm in size and the Fe/Si interface is smooth and sharp.

The topology of the top silicon and iron layer was formed by electron lithography on a Voyager (Raith) facility and liquid and dry etching. Anisotropic reactive-ion etching was performed using fluorine plasma generated from CF_4 gas on a Nordson MARCH RIE-1701 system. At the end of the technological process, the devices were examined by atomic force (AFM) and scanning electron microscopy (SEM) on a Hitachi TM-3000 microscope. Simultaneously, energy dispersive X-ray spectroscopy (EDS) elemental analysis was carried out. The transport properties of the active devices were studied on a Lakeshore EMPX-HF 2 cryogenic probe station at temperatures from 4.2 to 300 K using a Keithley 2634b two-channel source meter for direct current and an Agilent E4980A LCR meter for alternating current with frequencies from 20 Hz to 2 MHz. Additional conductivity measurements were performed using an original setup with a Keithley 2430 source meter and a Keithley Model 6517B electrometer/high resistance meter [13–15].

The devices were fabricated in several stages; the main ones are shown in Fig. 2a. A template that specified the device shape was developed using specialized software. The template was a set of images containing rectangles and circles serving as contact pads and bridges between them specifying the silicon current channel. The channel width varied within the row from 300 nm to 3 μm and the length (48 μm) was invariable. Next, a 300-nm-thick AZ 2035 nL negative electron resist layer was deposited onto the Fe/SOI structure surface by centrifugation followed by heat treatment at 112°C for 1.5 min. After that, the sample was exposed to an electron beam according to the specified template and one more heat treatment of the resist at a temperature of 112°C for 1.5 min was performed; the unexposed areas were washed off with PP-051MS developer. In this way, a chemically and mechanically stable mask was formed. Then, the sample was treated in an aqueous solution of hydrochloric acid to etch the Fe film. At this stage, the sample was intentionally overexposed in the solution to ensure the isotropic penetration of the acid under the mask to a depth of ~1 μm. This technique made it possible to dissolve iron in the bridge region and, at the same time, keep it on the contact pads. The exposure time was 50 s at 5-% concentration of an aqueous solution of hydrochloric acid. After that, the silicon layer was removed by dry reactive-ion etching using the same mask. In the above-described technological process, an array of silicon nanowires with metal contact pads formed from the iron film was obtained. Two contacts were formed on the device. The third contact was made by depositing indium onto the SOI substrate underside.

A SEM image of one finished device obtained in the EDS mode is shown in Fig. 2b. One can see drain–source contacts, a silicon bridge serving as the current channel of the transistor, and silicon oxide opened on the substrate after dry ion-plasma etching. The data

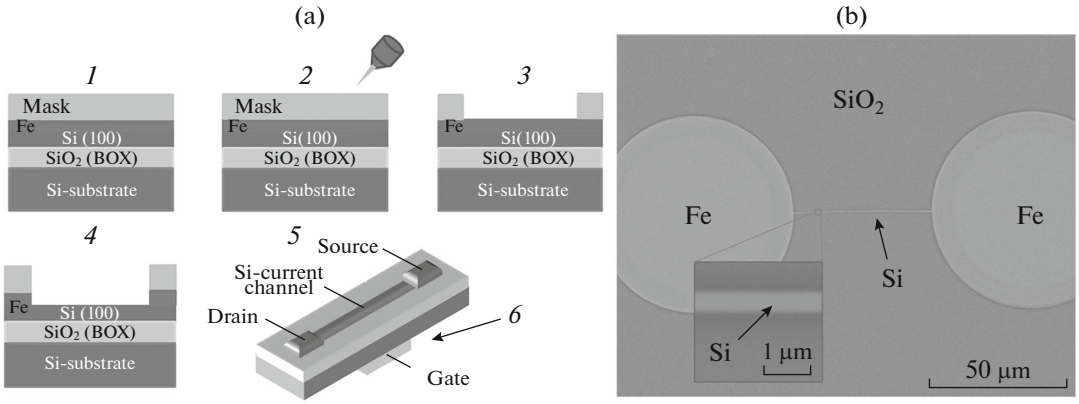

Fig. 2. (a) Schematic of fabrication of the nanowire device: (1) resist deposition, (*2*) exposure to an electron beam using a template, (*3*) resist development, (*4*) liquid chemical etching of Fe in a hydrochloric-acid solution, (*5*) reactive-ion etching of Si, (*6*) formation of the gate electrode. (b) SEM image in the EDS mode.

obtained allow one to estimate the wire thickness (~400 nm). The sizes were refined and compared with the template by the AFM technique. It was found that the wire width deviates from the mask by no more than 5%, while the height remains unchanged and amounts to 100 nm, which corresponds to the initial silicon layer thickness. This means that the mask reliably protects the device elements at the second etching stage.

RESULTS AND DISCUSSION

After fabrication, the electron transport properties of the nanowire devices were examined. Figures 3a and 3b show the transport and I–V characteristics of the device with a current channel width of 400 nm. Upon sweeping the voltage V_{GD} across the gate, the current I_{SD} in the channel sharply grows; i.e., the transistor is opened. The maximum ratio between the currents in the "on" and "off" transistor is five orders of magnitude. The characteristics of the device are ambipolar, i.e., almost independent of the gate polarity. This evidences the implementation of both n- and p-type conductivity. At a negative voltage V_{GD}, holes are accumulated; at a positive voltage V_{GD}, the inversion mode is activated, which was confirmed by the drain–gate C–V characteristics. Since the drain and source contacts are formed from iron directly on silicon with an impurity concentration of 10^{15} cm^{-3}, a Schottky barrier should form at the metal–semiconductor interface. Indeed, at zero gate voltage, the current in the transistor channel is very weak (below 10^{-10} A). This is due to the fact that the drain and the source are, in fact, two oppositely connected Schottky diodes and the current through such a structure is determined by the reverse branch of the I–V characteristic of the diode. In addition, as can be seen in Fig. 3b, at $|V_{GD}| > 0$, the drain–source I–V characteristics are, first, nonlinear and, second, different for positive and negative voltages V_{GD}.

Let us consider the processes occurring in the device. Upon sweeping the negative voltage V_{GD}, majority carriers (holes) are accumulated in the channel and, as a result, the Schottky barrier for holes significantly narrows and simultaneously decreases by means of the voltage V_{GD}. Thus, the current through the thin narrow Schottky barrier is supplemented by the tunneling current induced by thermionic emission. At a negative gate voltage, the inversion mode is implemented, i.e., minority carriers (electrons) are generated. In this case, all of the above reasoning remains true, but the conducting channel is formed by electrons. The difference between the drain–source I–V characteristics for different V_{GD} polarities is caused by the fact that, in the inversion mode, the current saturates due to the limited rate of the generation of minority carriers, which are electrons in boron-doped Si. At the same time, at a reverse bias V_{GD} in the accumulation mode, the hole current should increase in an unlimited way both in the case of thermionic emission and quantum-mechanical tunneling through the Schottky barrier, which is observed in the experiment.

As was mentioned above, devices with nanowire widths from 300 nm to 3 μm were fabricated and the transport characteristics were measured for all of them. All the features of the transport and I–V curves observed and described for the 400-nm-wide wire repeat for larger devices. Hence, it can be assumed that the main transport processes are independent of the transistor-channel width. However, analysis of the wire-width dependence of the ratio between the currents in the "on" and "off" transistor showed that the smallest device demonstrates the best performance (Fig. 3c). This is explained, first of all, by a significant decrease in the drain–source current in the narrow channel at zero gate bias. At the same time, at $|V_{GD}| = 15$ V, the drain–source current for the entire range of devices differs by only an order of magnitude. In other words, the current density, as expected, is almost inde-

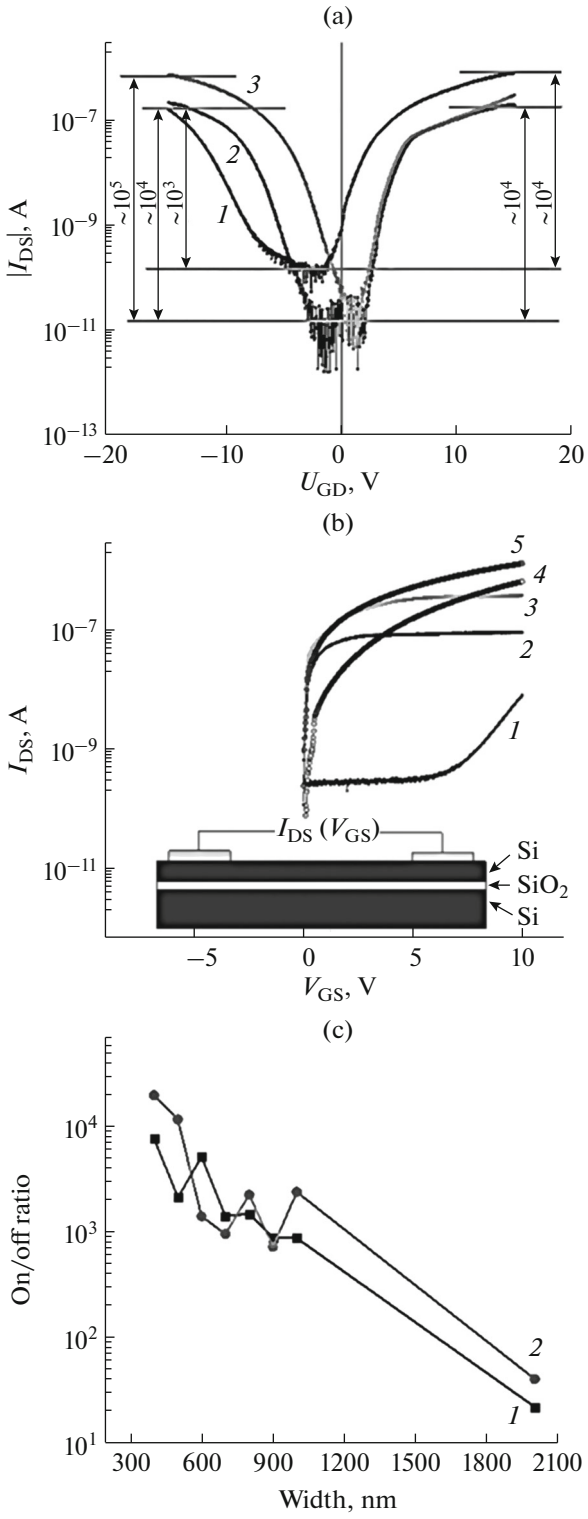

Fig. 3. (a) Bottom-gate voltage dependence of the drain–source current at a temperature of 300 K and a transport-channel width of 400 nm at drain biases of (*1*) −5, (*2*) 3, and (*3*) 7 V. (b) Drain–source *I–V* characteristics at gate biases of (*1*) 0, (*2*) 10, (3) 15, (4) −10, and (5) −15 V. Dependence of the ratio between the "on" and "off" transistor currents on the channel width at "on" voltages of (*1*) +15 and (*2*) −15 V.

pendent of the channel cross-sectional area in the "on" state. A decrease in the leakage current in the "off" state disproportionate to a decrease in the geometric sizes of the transistor can be attributed to the presence of defects at the metal–semiconductor interface. Such defects form localized energy states in the silicon band gap, the tunneling transport through which increases the inverse current through the Schottky barrier. The uneven distribution of defects can lead to the nonlinear dependence of their concentration in the metal–semiconductor contact area and, consequently, on the leakage current density. More specific findings require further investigations.

CONCLUSIONS

Thus, a simple technique for fabricating three-terminal devices, which are bottom-gate nanowire transistors, was proposed. The process includes single-layer electron lithography and liquid and dry etching. The structural characterization showed good accuracy, repeatability, and scalability of the developed technique. Studies of the electron transport properties showed that both *n*- and *p*-type conductivity is implemented in the device. At a negative voltage V_{GD}, holes are accumulated and, at a positive voltage V_{GD}, the inversion mode is activated. It was demonstrated that a Schottky barrier forms at the drain and source contacts and the transistor appears normally closed. All the features of the transport and *I–V* curves are repeated for all the fabricated devices. The maximum ratio between the currents in the "on" and "off" transistor (five orders of magnitude) is observed for the transistor with a current channel width of 400 nm. This is mainly due to a low leakage current in the narrow channel at zero gate bias. The proposed technique can be used to design and produce new electronic devices. Silicon nanowires have a small size comparable with the size of a molecule and a high surface area-to-volume ratio. These advantages, together with the low cost of the fabrication process, allow nanowire transistors to be used as ultrahigh-sensitivity electronic sensors. In sensing devices, a low voltage will effectively control the nanowire potential even at a very weak input signal, making this device highly sensitive, especially for chemical probing and biosensing.

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