physica status solidi a
www.pss-a.com

Effect of Magnetic and Electric Fields on the AC Resistance of a Silicon-on-Insulator-Based Transistor-Like Device

Dmitry Smolyakov, Anton Tarasov, Lev Shanidze, Ilya Bondarev, Filipp Baron, Anna Lukyanenko, Ivan Yakovlev, Mihail Volochaev, and Nikita Volkov*

Herein, the AC magnetoresistance (MR) in the silicon-on-insulator (SOI)-based Fe/Si/SiO_2/p-Si structure is presented. The structure is used for fabricating a back-gate field-effect pseudo-metal–oxide–semiconductor field-effect transistor (MOSFET) device. The effects of the magnetic field and gate voltage on the transport characteristics of the device are investigated. Magnetoimpedance value of up to 100% is obtained due to recharging of the impurity and surface centers at the insulator/semiconductor interface. A resistance variation of up to 1000% is found, which is caused by the voltage applied to the gate and the field effect on the band structure of the sample. Combining the magnetic and electric fields, one can either change the absolute value of the AC resistance while having the MR fixed or change the sign and character of the field dependence of the MR. The observed effects can be used in the development of magnetic-field-driven SOI-based devices and high-frequency circuits.

1. Introduction

Semiconductor structures may be legitimately called the basis of today's electronics. They are widely used in various fields, including nanoelectronics,[1] nanophotonics,[2] optoelectronics,[3] and biosensorics.[4] The use of semiconductors makes it possible to create new electronic devices and improve existing ones, reduce their dimensions and power consumption, and enhance their efficiency, speed, and reliability. In modern electronics, nanostructures are highly demanded for downsizing the semiconductor devices and their fabrication is congenial with the silicon-on-insulator (SOI) technology,[5] which benefits the metal–oxide–semiconductor field-effect transistor (MOSFET) in terms of high channel mobility, low parasitic capacitance, and so on. The conventional Si substrates are not so effective at gate lengths shorter than 100 nm due to various off-state leakage currents.[6] In addition, the replacement of the Si substrates with SOI structures improved the scalability and electrostatic parameters.[7] In due time, the introduction of SOI technology mitigated the charge density problems typical for the conventional MOSFETs.[8] As metal–oxide semiconductors are widely used in thin-film transistors,[9] an important task for researchers is to improve their characteristics. The aforesaid has stimulated our interest in studying the SOI-based semiconductor transistors.[10] Here, we demonstrate the effect of magnetic and electric fields on the transport properties of a Fe/SOI structure, which represents a back-gated transistor-like device structure with source/drain Schottky contacts. In the literature, this device is known as pseudo-MOSFET.[11]

2. Experimental Section

We fabricated a Fe/SOI structure and used it as a basis of a back-to-back Schottky diode device. A polycrystalline iron film was thermally evaporated onto the SOI structure with a boron-doped Si(100) device layer with a resistivity of 18 Ω cm. Before placing into a growth chamber, the substrates were chemically cleaned.[12] Prior to the evaporation of iron, they were annealed in ultrahigh vacuum (a residual pressure of 10^{-8} Pa) at a temperature of 400 °C for 30 min to clean the Si surface. **Figure 1**a shows the cross-sectional transmission electron microscopy (TEM) images of the structure. It can be seen that the structure layers are fairly smooth with well-resolved borders without interdiffusion. The final structure consists of handling Si, a 200 nm-thick buried oxide (BOX) layer, a 100 nm Si device layer (SOI), and a 14 nm-thick iron film. The obtained structure was used to fabricate the pseudo-MOSFET device by a combination of optical

D. Smolyakov, A. Tarasov, L. Shanidze, I. Bondarev, F. Baron, A. Lukyanenko, I. Yakovlev, M. Volochaev, N. Volkov
Kirensky Institute of Physics
Krasnoyarsk Scientific Center
Siberian Branch
Russian Academy of Sciences
Akademgorodok 50, bld. 38, Krasnoyarsk 660036, Russia
E-mail: sda88@iph.krasn.ru

A. Tarasov, A. Lukyanenko
Institute of Engineering Physics and Radio Electronics
Siberian Federal University
pr. Svobodny 79, Krasnoyarsk 660041, Russia

L. Shanidze, I. Bondarev
Krasnoyarsk Scientific Center
Siberian Branch
Russian Academy of Sciences
Akademgorodok 50, Krasnoyarsk 660036, Russia

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/pssa.202100459.

DOI: 10.1002/pssa.202100459

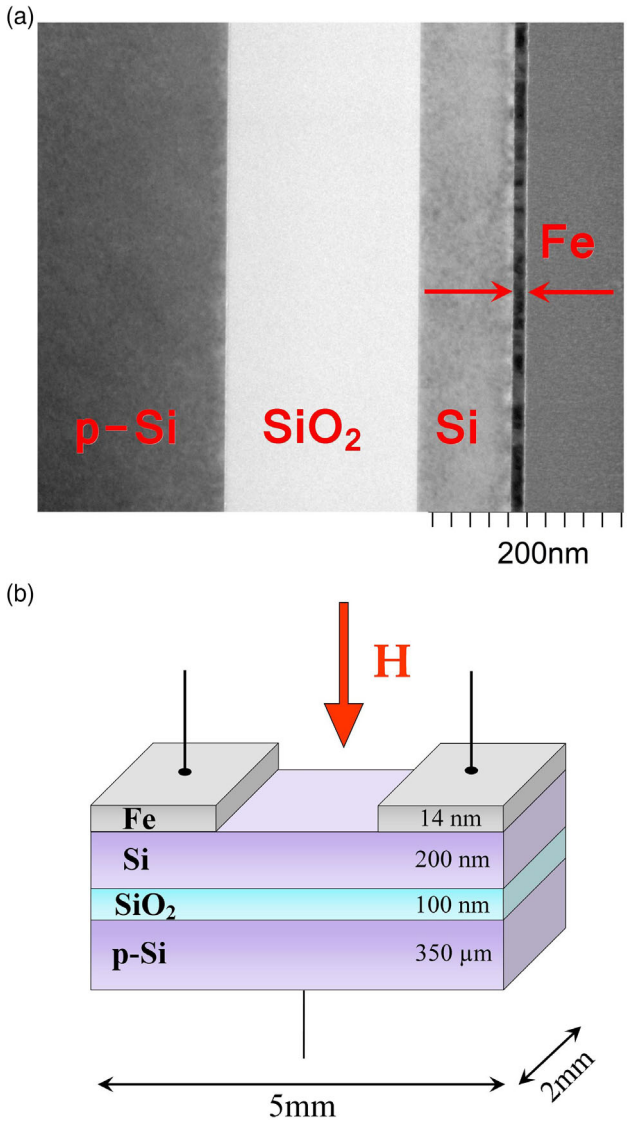

Figure 1. a) Cross-sectional TEM images of the SOI structure; b) schematic of the device.

lithography and wet etching in nitric acid (HNO_3). The metallic film was etched in the center (Figure 1b) to form two metal contacts on the Si device layer surface. Using the silver epoxy we processed two front electric contacts on the iron film and placed one contact at the back of the silicon substrate. In the fabricated pseudo-MOSFET the iron metal contacts functioned as source and drain, while the silicon substrate served as a back gate. The contact pad area was 1 mm^2. Fe contact separation distance was 1 mm. A schematic of the device is shown in Figure 1b. The DC transport properties of the fabricated pseudo-MOSFET were examined using a Keithley 2634b dual channel source meter. The AC measurements were conducted on an Agilent E4980A LCR meter. During the AC measurements, the current frequency was varied from 20 Hz to 2 MHz, AC drain voltage was 0.1 V, and the DC voltage applied to the gate was swept from –10 to 10 V. The measurements were performed in the temperature range from 5 to 270 K and in an external magnetic field up to 0.8 T.

3. Results and Discussion

Our studies were motivated mainly by the widespread use of semiconductor materials in modern electronics, namely, in processing the structures with complex topology such as transistors. In view of this, the study of the transport properties of the structure began with DC measurements of both the back gate–drain (**Figure 2**a) and drain characteristics (Figure 2b).

As can be seen from Figure 2a, when sweeping the back gate voltage, there is a sharp increase in the channel current, which is a signature of transistor turn-on. The drain characteristics are nonlinear (Figure 2b). Observed characteristics demonstrate typical behavior for fully depleted SOI devices. Moreover, we can clearly observe the difference in the behavior of the device when a voltage U_g of different polarity is applied to the gate, which shows that both n- and p-type conductivity is realized.

In our device, the SOI substrate acts as a back gate. This means that by applying voltage to the SOI we can choose the type of carriers (electrons or holes) that forms the conducting channel of the transistor.[13] As the drain and source contacts are made of

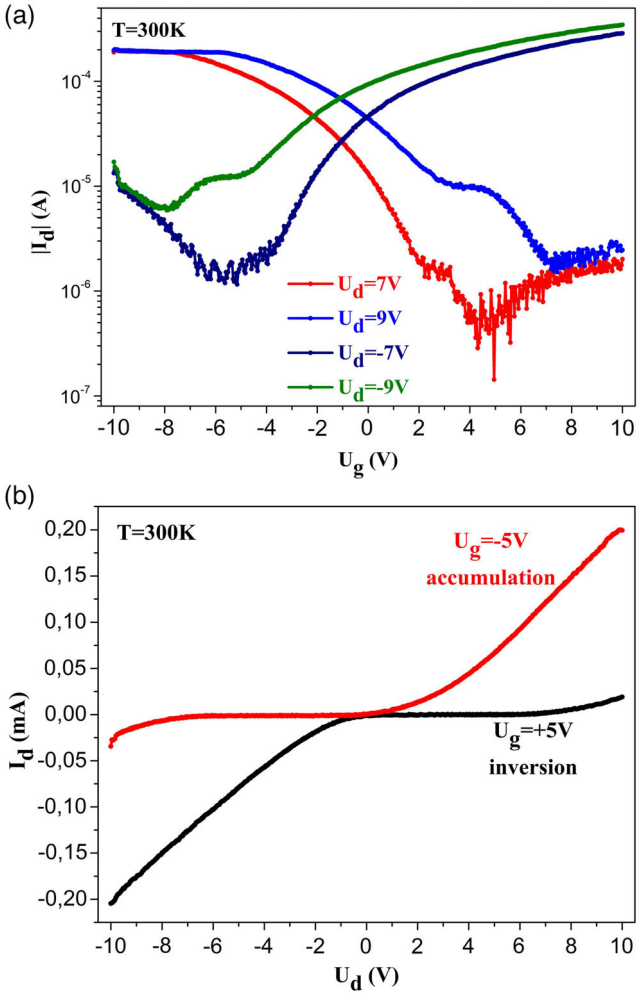

Figure 2. a) Dependence of the drain current I_d on gate voltage U_g at different source–drain voltages. b) Drain characteristics at different gate voltages.

iron directly on silicon with an impurity concentration of 10^{15} cm^{-3}, there is a Schottky barrier in the region of the source and drain contacts and terminals with p-Si (**Figure 3**a). At negative U_g values the majority carriers (holes) are accumulated in the channel; as a result, the Schottky barrier for holes narrows and simultaneously lowers if the drain–source voltage U_{sd} is applied. As a result, the tunneling component is added to the thermionic emission-induced current through the thin and narrow Schottky barrier. The so-called accumulation mode of the major carriers is thus implemented. If a positive voltage is applied to the gate, the inversion mode is realized, i.e., minority carriers (electrons) are generated. In this case, the aforementioned reasoning is still valid; however, the conducting channel is formed by electrons. The main difference between the modes is that, in the inversion mode, the current saturates due to the limited rate of generation of minority carriers (for p-Si, these are electrons).

Similar measurements were conducted in the AC mode. Figure 3b shows the real part of the impedance R as a function of the gate voltage U_g. It can be seen that the curve significantly changes only at voltages higher than 4 V. These features are caused by opening of the transistor. When $U_g > 4$ V in the transistor channel, the inversion layer is formed with high electron concentration resulting in significantly lower R.

In applied magnetic field of 0.8 T, the resistance increases by a factor of 5. In the AC measurements we can trace the changes in the transport characteristics upon variation in the current frequency f. **Figure 4**a shows that the change in the behavior of the $R(f)$ curves is only observed in the frequency range of up to 100 kHz. Around 1 kHz, there are features typical for the systems governed by the Debye relaxation processes. Such features were already observed for a metal-insulator-semiconductor (MIS) structure and were attributed to the presence of characteristic times

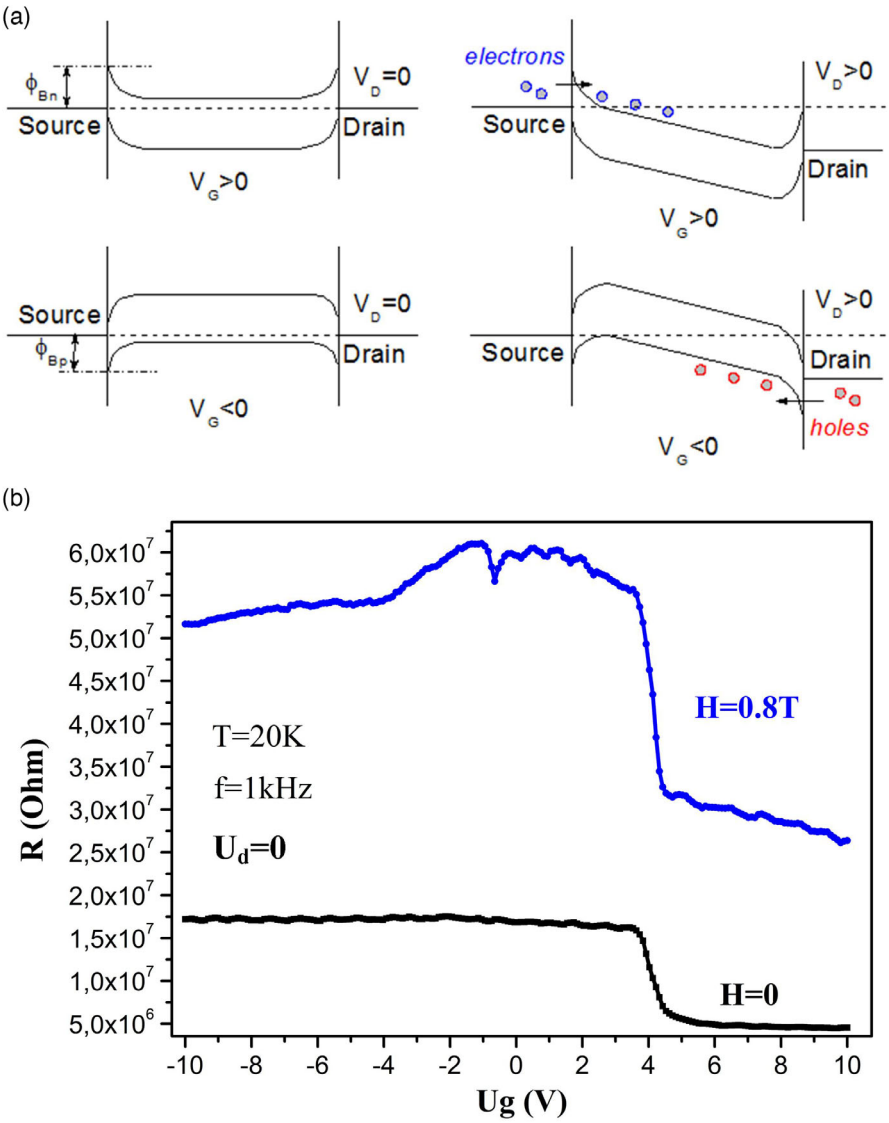

Figure 3. a) Band diagram illustrated the principle of operation of a back-gate device with source/drain Schottky contacts. b) Dependence of the real part of impedance R on gate voltage U_g in a magnetic field of $H = 0.8$ T and at $H = 0$.

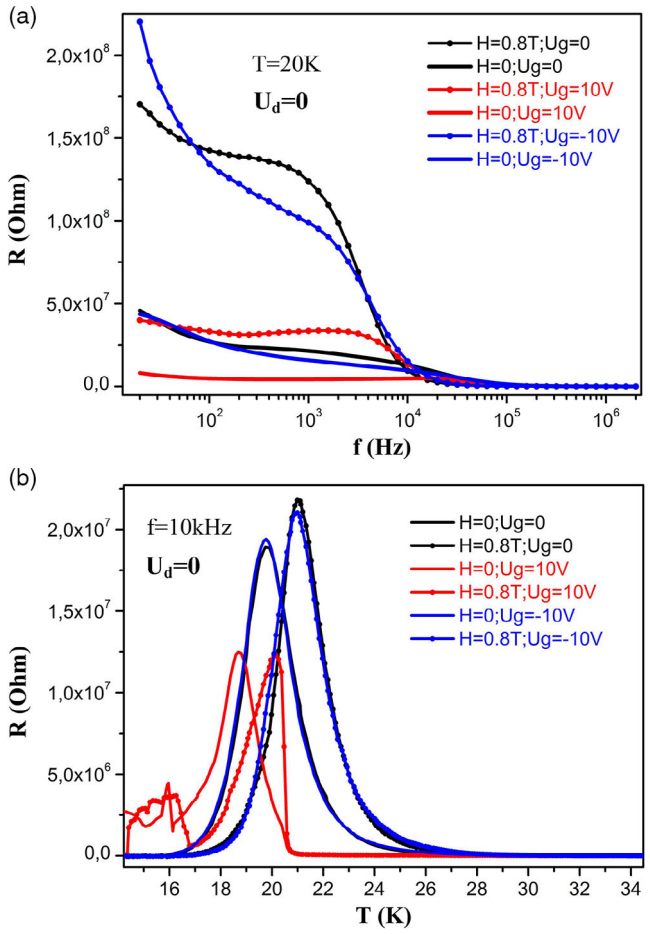

Figure 4. Dependence of the real part of impedance R on a) AC frequency f at $T = 20$ K and b) temperature at different variations of the effect of magnetic fields of $H = 0$ and 0.8 T and gate voltages of $U_g = 0$, 10, and –10 V.

of recharging of the impurity and surface centers.[14–16] It is the recharging processes that lead to the occurrence of the features in the form of peaks in the $R(T)$ curves (Figure 4b). In addition, the effect of the gate voltage U_g can be noted. The behavior of the frequency dependences significantly changes only at $U_g = +10$ V, which is consistent with the $R(U_g)$ curves in Figure 3b.

These $R(T)$ peaks appear due to the presence of impurity centers involved in the carrier emission/capture processes. The impurity centers are located at the Fe/silicon interface. At a certain temperature, when Fermi level E_F starts crossing energy levels E_S of the surface states, AC bias U_{ac} across the structure modulates the position of E_S relative to E_F, thereby initiating the capture/emission of electrons from the interface states to the valence band (**Figure 5**).

The appearance of the impedance or admittance singularities is well known in admittance spectroscopy, which is based on the measurements of the real part of the complex admittance $Z = R + iX$ at frequencies and temperatures ensuring the rate of carrier emission from traps comparable with the measuring frequency.[17] The peak in the $R(T)$ dependence should occur under the condition $\omega\langle\tau_0\rangle = 1$ where $\omega = 2\pi f$ is the angular frequency of U_{ac} and $\langle\tau_0\rangle$ is the average relaxation time, which characterizes the process of charging–discharging the interface states.

Under the action of magnetic field H this peak shifts toward higher temperatures. The shift is about 2 K in a magnetic field of 0.8 T. The effect of the magnetic field is related to the shift of the energy levels of the interface states relative to the semiconductor band edges toward higher energies (to the bandgap center). Previously, we described a similar phenomenon.[18] However, the voltage applied to the gate also affects the behavior of these features. When a negative voltage of $U_g = -10$ V is applied, no changes in the features are observed. When U_g is positive, the $R(T)$ peaks shift toward lower temperatures. Previously,[19] we described in detail the effect of bias in similar structures. In our case, the gate, along with its basic role, acts as a source of bias in the impedance measurements. The results of switching-on the gate voltage can be most easily explained using the band diagram (Figure 5).

The energy levels of the impurity centers are pinned to a certain point in the semiconductor bandgap. Upon variation in the bias U_g across the MIS structure, the positions of the energy levels of the interface states change according to the shift of the semiconductor bandgap edges, while the Fermi-level position E_F remains fixed. Under the reverse bias, the $R(T)$ peaks shift toward lower temperatures, which is reflected in the band diagram as a shift in the E_S level (red dashed line in Figure 5b. The negative bias did not noticeably affect the behavior of the curve (Figure 5a). The latter is probably due to the fact that, under the forward bias, the main potential drop occurs in the bulk of the semiconductor rather than in the MIS junction. The effect of the magnetic field can be explained assuming that it shifts the energy levels of the interface states (and the acceptor levels as a whole) relative to the semiconductor band edges toward higher energies (to the bandgap center). In addition, U_g does not change the distance between E_S and band edges. However, the band bending at the interface between the semiconductor and the metallic layer, as well as U_g, changes the distance between E_S and E_F.

At the same time, one may note an abrupt drop of the peak in the switched-on magnetic field (Figure 4b). This is apparently due to the fact that, in the inversion mode, the Fermi level hits the conduction band with an increase in temperature until the end of the carrier emission/capture processes. This leads to an abrupt termination of this process and carriers start flowing from the semiconductor directly into the metal, reducing the impedance of the structure by three orders of magnitude. This behavior of the features causes a peculiar change in the $R(H)$ curves (**Figure 6**a).

Indeed, analyzing the $R(H)$ dependences, we can note that at a temperature of 21 K applying a voltage of $U_g = -10$ V does not change them, while at $U_g = +10$ V the resistance decreases by up to three orders of magnitude. The form of the field dependences depends on a portion of the feature (peak) in Figure 4b observed at a specified temperature (the peak slope or the peak top). Thus, the field dependences can take the form of one or two bulges.

Due to these electron transport features we can observe the magnetoresistance (MR) (Figure 6b). In the AC mode, at a gate voltage of $U_g = 0$ or –10 V, we can observe values of the MR = 100*((R(H) – R(0))/R(0)) of up to 100%. Here, the MR

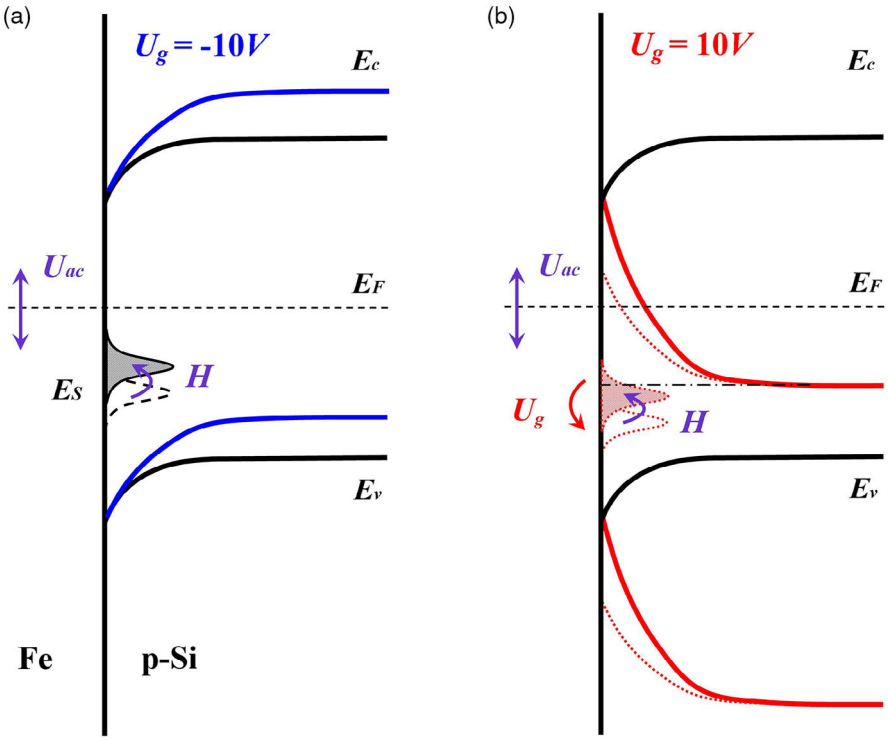

Figure 5. Schematic band diagram of the sample. Black lines demonstrate unbiased metal/p-Si Schottky contact. E_F is the Fermi level, E_S is the impurity level, H is the magnetic field, U_{ac} is the applied AC voltage, and U_g is the gate voltage. U_g = a) –10 V and b) 10 V.

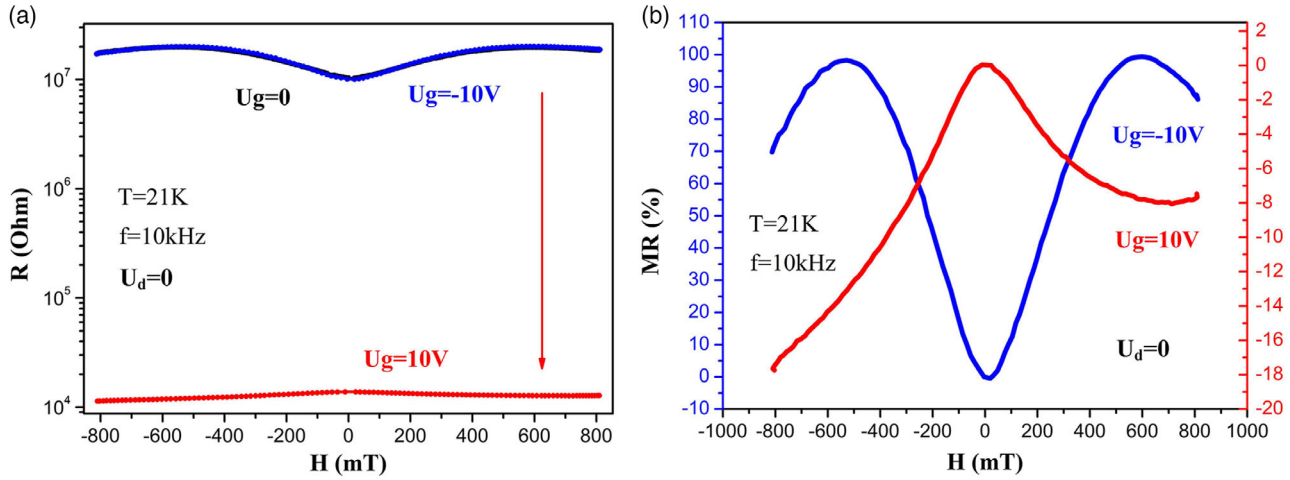

Figure 6. a) Field dependence of the real part of impedance $R(H)$ at different gate voltages U_g. b) MR at U_g = 10 and –10 V.

is caused by recharging of the impurity and surface centers at the insulator/semiconductor interface. At $U_g = +10$ V, the changes in the R value can attain 1000% because the Fermi level hits the conduction band in the inversion mode and the emission/capture processes are abruptly terminated. In this case, the MR value reaches 20%; however, the MR sign and the character of the field dependence change.

4. Conclusions

Thus, the AC transport characteristics of the SOI-based Fe/Si/SiO_2/p-Si structure were investigated. The Fe film was deposited onto the SOI structure and etched in the center. The obtained pseudo-MOSFET device had two contacts on the metallic film and one contact on the silicon substrate. The AC measurements

revealed the effect of a magnetic field on the transport properties. The temperature dependences exhibited some features below 40 K. In the applied magnetic field and gate voltage, these features shifted toward higher or lower temperatures, respectively. This was attributed to the impact of the field effect on the band structure. These effects cause the occurrence of the MR. MR values of up to 100% were observed, which is caused by recharging of the impurity and surface centers at the metal/semiconductor interface. Moreover, when the gate voltage was switched, a change in the R value attaining 1000% was found, which is induced by the abrupt termination of the emission/capture processes and the carrier flow directly from the semiconductor into the metal. At the same time, the MR value remains invariable, while the shape of the MR curve changes due to the change in the positions of the features in the temperature dependence. It can be concluded that using a magnetic field, one can obtain an AC MR of up to 100%. Via changing the gate voltage, one can change the absolute value of the resistance, the shape of the curve, and the MR sign. Such devices may potentially be useful for magnetic electronics or high-frequency SOI-based circuits.

Acknowledgements

The authors thank the Krasnoyarsk Territorial Center for Collective Use, Krasnoyarsk Scientific Center of the SB RAS, for electron microscope investigations. This study was supported by RFBR, Krasnoyarsk Territory and Krasnoyarsk Regional Fund of Science, projects nos. 20-42-243007 and 20-42-240013, and by the Government of the Russian Federation, the Mega-grant for the Creation of Competitive World-Class Laboratories, agreement no. 075-15-2019-1886.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

impurities states, magnetoimpedance, magnetoresistance, pseudo-MOSFET, semiconductors, SOI structure, transistor

Received: July 14, 2021
Revised: October 12, 2021
Published online:

[1] O. Bubnova, *Nat. Nanotechnol.* **2017**, *1*, 2.
[2] F. Xia, H. Wang, D. Xiao, M. Dubey, A. Ramasubramaniam, *Nat. Photonics.* **2014**, *8*, 899.
[3] F. Priolo, T. Gregorkiewicz, M. Galli, T. F. Krauss, *Nat. Nanotechnol.* **2014**, *9*, 19.
[4] A. Tereshchenko, M. Bechelany, R. Viter, V. Khranovskyy, V. Smyntyna, N. Starodub, R. Yakimova, *Sens. Actuators B Chem.* **2016**, *229*, 664.
[5] M. I. Current, S. W. Bedell, I. J. Malik, L. M. Feng, F. J. Henley, *Solid State Technol.* **2000**, *43*, 66.
[6] J. P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, Springer US, **1997**, p. 67.
[7] C. K. Pandey, D. Dash, S. Chaudhury, *ECS J. Solid State Sci. Technol.* **2018**, *7*, 59.
[8] K. Suzuki, S. Pidin, *IEEE Trans. Electron Devices* **2003**, *50*, 1297.
[9] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature*, **2004**, *432*, 488.
[10] D. A. Smolyakov, A. S. Tarasov, I. A. Yakovlev, M. N. Volochaev, *Semiconductors* **2019**, *53*, 1964.
[11] V. P. Popov, V. A. Antonov, M. A. Ilnitsky, I. E. Tyschenko, V. I. Vdovin, A. V. Miakonkikh, K. V. Rudenko, *Solid-State Electronics* **2019**, *159*, 63.
[12] A. Ishizaka, Y. Shiraki, *J. Electrochem. Soc.* **1986**, *133*, 666.
[13] S. M. Koo, M. D. Edelstein, Q. Li, C. A. Richter, E. M. Vogel, *Nanotechnology* **2005**, *16*, 1482.
[14] X. K. Li, W. J. Ji, J. Zhao, S. J. Wang, C. T. Au, *Journal of Catalysis* **2005**, *236*, 181.
[15] M. Ulusoy, Ş. Altındal, P. Durmuş, S. Özçelik, Y. Azizian-Kalandaragh, *J. Mater. Sci.: Mater. Electron.* **2021**, *32*, 13693.
[16] M. H. Al-Dharob, A. Kökce, D. A. Aldemir, A. F. Özdemir, Ş. Altındal, *J. Phys. Chem. Solids* **2020**, *144*, 109523.
[17] A. R. Peaker, V. P. Markevich, J. Coutinho, *J. Appl. Phys.* **2018**, *123*, 161559.
[18] D. A. Smolyakov, A. S. Tarasov, M. A. Bondarev, A. A. Nikolskaya, V. K. Vasiliev, M. N. Volochaev, N. V. Volkov, *Mater. Sci. Semicond.* **2021**, *126*, 105663.
[19] N. V. Volkov, A. S. Tarasov, D. A. Smolyakov, A. O. Gustaitsev, M. V. Rautskii, A. V. Lukyanenko, M. N. Volochaev, S. N. Varnakov, I. A. Yakovlev, S. G. Ovchinnikov, *AIP Adv.* **2017**, *7*, 015206.