ИНСТИТУТ ЯДЕРНОЙ ФИЗИКИ
им. Г.И. Будкера СО РАН

A.R. Frolov, T.V. Oslopova and Yu.N. Pestov

DOUBLE THRESHOLD DISCRIMINATOR FOR TIMING MEASUREMENTS

BudkerINP 94-31

НОВОСИБИРСК

DOUBLE THRESHOLD DISCRIMINATOR FOR TIMING MEASUREMENTS

A.R.Frolov, T.V.Oslopova and Yu.N.Pestov

Budker INP,
630090 Novosibirsk, Russian Federation

Abstract

The new type of a discriminator is based on the idea of simultaneous time measurements at two different thresholds for each pulse. Instead of using of two independent electronic TDC channels this discriminator produces an output pulse with the timing taking into account the information from two time measurements "on-line". The operation principle, analytical calculations and experimental results are presented. The time walk of the discriminator at the level of 10 ps at the range of the input pulse height of 0.2–1.5 V has been obtained.

1. Introduction

The Pestov spark counter [1] has been proposed as a base for the TOF system at the ALICE detector, CERN [2]. The time resolution of this TOF system should be at the level of 40–70 ps at the total number of counter channels about 170000. Taking into account the large number of channels, each component of the channel electronics must be cheep. In this paper we suggest one of a possible decision of the discriminator problem.

Pulses from the spark counter prototype for the TOF system had a rise time better than 300 ps, a pulse decay of few nanoseconds and an amplitude of 0.3–0.5 V [3, 4]. The width of a pulse height distribution of ±50% has been a result of a discharge fluctuation (±30%) and a different position of a spark relatively to pick-up electrodes (±30%).

The time walk due to the input threshold crossing time should give an electronic resolution at the level of 15 ps at a discriminator threshold of 30 mV. In early works [1, 3] good timing characteristics of the spark counter with a home made leading edge discriminators (LED) based on tunnel diodes have been obtained. Unfortunately, this type of a discriminator is not promising for the VLSI technology, which is planned to be used for the TOF electronics. The test of standard LED's (LeCroy 620, LeCroy 623 and GSI 8001) with spark counter prototype pulses as well as also with generator pulses gave the electronic time resolution of 70 ps only [4]. Therefore the intrinsic response time of these models of LED's is too bad for this application.

In the MARK III detector at SLAC the electronic resolution was improved by simultaneous timing measurements at two different thresholds for each pulse [5]. Following software calculations in principle allow to obtain a start of each pulse taking into account the input-to-output voltage transfer curve of LED's. Disadvantages of this method are necessity of software calculations and increasing of a number of TDC electronic channels in two times.

The new type of a discriminator described in the paper realizes the previous idea in one element. The discriminator makes two timing measurements and produces an output pulse taking into account the information from these measurements "on-line". At this case the number of TDC channels of the TOF system is minimum.

It is necessary to mention two other designs of a discriminator, which could be in principle used: 1) a picosecond resolution state-of-the-art voltage comparator [6], which has a good timing but is very expensive now and 2) a constant fraction discriminator [7], which is ineffective with spark counter pulses mainly because their shape verifies essentially [3, 4].

2. Operation principle and analytical calculations

The block diagram of the double threshold discriminator (DTD) is shown in Fig. 1. This topology comprises three comparators. Two input comparators with different thresholds have current outputs connected to integrating capacities $C1$ and $C2$. A potential difference from the capacities is applied to the input of the third comparator. The current and capacity values were chosen to get the right timing (see section 2.1) of an output pulse.

2.1 The time walk of the DTD with an input ramp

A principle of choosing of the current and capacity values at this case is illustrated in Fig. 2. Fig. 2,*a* shows two input pulses with different amplitudes U_{i1} and U_{i2}. When an input amplitude U_{i1} exceeds the U_1 threshold at the moment of t_{11}, current I1 at the output of the first comparator appears and voltage on capacity $C1$ starts to change with time. Current I_2 at the output of the second comparator appears when an input amplitude U_{i1} exceeds the U_2 threshold at the moment t_{21}. The time dependence of the potential difference at the capacities is shown in Fig. 2,*b* assuming that the response time of comparators is equal to the input threshold crossing time (ideal comparator). When potential difference at the input of the third comparator is equal to its threshold, U_3, an output pulse from the DTD appears.

The timing T_0 (Fig. 2,*b*) for amplitudes U_{i1} and U_{i2} coincides if an equation

$$U_2/U_1 = (I_1/I_2) \times (C2/C1) \tag{1}$$

is valid. Hence the DTD on the base of ideal comparators has the "zero" time walk for an input ramp with any amplitude value and a rise time.

In practice, an input comparator is not ideal and its time walk includes the input threshold crossing time and the intrinsic response time. Obviously, a constant propagation delay in comparators does not influence the time walk of the DTD changing its delay time only.

A principle of the full compensation of the input threshold crossing time by the DTD for a ramp is based on a linear dependence of this time on an inverse input amplitude. If the intrinsic response time of a comparator is also proportional to an inverse pulse amplitude, the time walk of a comparator could be completely compensated by the DTD for a ramp. This compensation could be achieved by changing one (or few) circuit parameter from values optimized for a ramp (1).

Luckily the time walk function of real comparators is falling down with amplitude increasing. Therefore the input in the DTD time walk from the intrinsic response time of real comparators should be essentially compensated by the DTD.

2.2 The time walk of the DTD with an exponential waveform of an input pulse

If the front of an input pulse differs from a ramp, the time walk of the DTD, based on ideal comparators, depends on a waveform and a ratio of two thresholds $\alpha = U_2/U_1$. Fig. 3 shows the results of analytical calculations of the DTD time walk with an input waveform of

$$U = U_{i0} \cdot (1 - \exp(-t/t_0)) \tag{2}$$

at different α, where to is a pulse rise time. For each α the circuit parameters were optimized for a ramp (1). The calculated characteristic improves with α decreasing. However, from experiments with the real DTD we have found influence of a fluctuation of the I_1 and I_2 currents on timing stability of a third comparator output pulse at α less than 3.

The time walk of the DTD for a (2) waveform (Fig. 3) could be improved by changing the circuit parameters (U_1, U_2, I_1, I_2, C1 or C2) from values optimized for a ramp (1). As an example Fig. 4 shows the calculated DTD time walk at different threshold values of U_2. Other circuit parameters were fixed and they coincided with the values for a ramp at the input threshold ratio of $\alpha = 3$. At U_2 less than the value optimized for a ramp, the DTD time walk curves cross the amplitude axis (Fig. 4). Time diagrams on Fig. 5 illustrate choice of the U_2 value so as a time walk curve would cross the amplitude axis at a definite input amplitude. In Fig. 5,*b* the (1) straight line corresponds to potential difference at the input of the third comparator for an input ramp, the (2) straight line — for a (2) waveform. Decreasing U_2 threshold it is possible to combine these two lines and obtain for a U_{io} input amplitude the same timing, T_0 as for a ramp.

3. Circuit details and experimental results

3.1 Logic of work of the DTD based on a K1500LP114 circuit

A commercially available K1500LP114 integrated circuit with an emitter-coupled logic [8] has been used at the DTD (Fig. 1). Similar parameters are characteristic of a MECL100114 circuit [9]. Both circuits are a quint differential line receiver. Each receiver consists of one differential amplifier and an emitter-follower buffer.

The differential amplifier of the comparator at the DTD (Fig. 1) was used as a threshold element. An emitter-follower provided a fast set of the initial voltage on the capacitors C1 and C2 (Fig. 1) at an absence of an input signal. When an input signal triggered differential amplifiers, an emitter-follower switched off the amplifier outputs from the capacities C1 and C2. After that the working cycle of the DTD started (see section 2.1). A formula (1) is valid for this DTD circuit if the U_4 voltage value is much higher than an output comparator threshold value, U_3 (Fig. 1). It is important that according to analytical calculations the DTD with an input ramp provides the right timing also for comparable values of U_3 and U_4 if

$$U_2/U_1 = (R2/R1) \times (C2/C1) \tag{3}$$

An equation (3) coincides with (1) for $U_4 >> U_3$.

3.2 Comparator characteristics

The gain of about 25 was obtained from the input-to-output static characteristic of a K1500LP114 comparator, which extends from U_{cthr}=15 mV to U_{csat}=42 mV at the input and U_{cL}=0.75 V and U_{cH}=1.5 V at the output

(Fig. 6). The output timing is specified as the time, tref at which the output signal crosses an arbitrary value U_{ref} the mid point of the response curve as shown in Fig. 6. The threshold of the input comparator is equal to the sum of Uref and an external bias voltage.

Fig. 7 shows the time walk of the comparator at a threshold of 30 mV measured with a mercury generator (Tektronix 519-PII, serial 94780) at a pulse rise time of 0.2 ns and with a russian model G5-78 pulse generator at a pulse rise time of 0.8 and 1.3 ns. The curves with an input pulse rise time of 0.2 and 0.8 ns coincide practically and hence at this case the time walk is determined by an intrinsic response time of the comparator.

3.3 Circuit details

In the tested DTD next parameters of circuit elements were used: C1=18 pF, C2=24 pF, R1=415Ω, R2=544Ω and R3=50Ω. An external voltage source was equal to 4.5 V.

The U_1 threshold of the first input comparator of the tested DTD was equal to $U_1 = U_{ref} \cong 30$ mV. The U_2 threshold of the second input comparator was adjusted to obtain the best time walk characteristic of the DTD. A resistance of 30Ω, used as a U_3 voltage source (see Fig.1), provided the U_3 threshold value of 150 mV.

These circuit parameters provided the time walk compensation for input pulses with a rise time up to 1.5 ns.

A length of an output pulse from the DTD was determined by a length of an input pulse. An emitter-follower in the output comparator provided an output signal with an amplitude of 0.8 V on a load of 50Ω.

3.4 Experimental results

Fig.8*a* shows the time walk of the DTD at the input thresholds of U_1=30 mV and U_2=86 mV with a pulse rise time of 0.8 and 1.3 ns from a russian model G5-78 pulse generator. The time walk of the DTD at U_1=30 mV and U_2=76 mV are shown in Fig.9*a*. From these two figures we can estimate an experimental sensitivity of a maximum value of the time walk curve to changing the U_2 threshold value — about 2 ps/mV.

The measured DTD time walk did not depend on a length of an input pulse, t_i at least at $t_i > 3$ ns. This result coincides with the operation principle of the DTD.

The measured delay time of the DTD was 5 ns. This value coincides practically with the sum of a delay time of two comparators (2x1.5 ns [8]) and the calculated capacitor decay time of about 2 ns. The effect of temperature on delay time of the DTD was measured at a temperature range of 15–35 C. The average temperature delay time coefficient of 0.7 ps/deg.cent. has been obtained.

4. Discussion

The analytical calculations of the time walk of the DTD were done for ideal comparators and ideal elements of the circuit. The real waveform of input pulses from a generator could also differ from a (2) formula, which was used for the calculation. Nevertheless a good coincidence of the measured data (Fig $8a, 9a$) with the calculations (Fig.$8b, 9b$) was obtained:

a) The measured time walk curves repeat the shape of the calculated ones.

b) According to the calculations the time walk function of the DTD, is proportional to a rise time of an input pulse (Fig.3, 4, $8b, 9b$). The experimental results (Fig.$8a, 9a$) confirm qualitatively this prediction.

c) The dependence of the time walk on aU_2 threshold value is also similar for measured and calculated data.

According to our understanding of the operation principle of the DTD, this coincidence is the result of a compensation by the DTD of the intrinsic response time of comparators and nonideality of the circuit elements.

5. Conclusion

The realization of the double threshold discriminator became possible due to two reasons. Firstly, it was found the simple design of the time walk compensation circuit allowing with ideal electronics to get in principle the zero time walk for the input ramp. Secondly, it was shown that this circuit compensates essentially the time walk of $aK1500LP114$ comparator.

The time walk of the DTD on the level of $10ps$ at the range of an input pulse amplitude of $0.2 - 1.5V$ has been obtained. This characteristic is good enough for an application at the TOF system for the ALICE detector. It is important that the circuit of the DTD could be manufactured in the VLSI technology.

References

1. *V.V. Parhomchuck, Yu.N.Pestov and N.V.Petrovykh.* Nucl. Instr. and Meth. 93 (1971) 269.
2. Letter of Intent for ALICE, CERN/LNCC/93-16, 1993.
3. *Yu.N.Pestov.* Exper. Apparatus for High Energy Particle Physics and Astrophysics, 4th San Miniato Topical Seminar, World Sientific, (1991), 156.
4. *H.R.Schmidt.* TOF, Internal Note ALICE 93-36, November 1993.
5. *D.Bernstein et al.* Nucl. Instr. and Meth. A226 (1984) 301-318.
6. IEEE Transaction on nuclear science, vol.37, No.2. April 1990, 424-429.
7. *E.A.Meleshko.* Nanosekundnaia Electronika, Moskva, Energoatomizdat, 1987.
8. Microchemy integralnye narodnohoziastvennogo naznacheniia. Sbornik spravochnyh listov, RNII Elektrostandart, RD 11 0435.6-91.
9. Integrated circuits, PHILIPS, Data handbook, Book IC08, 1986.

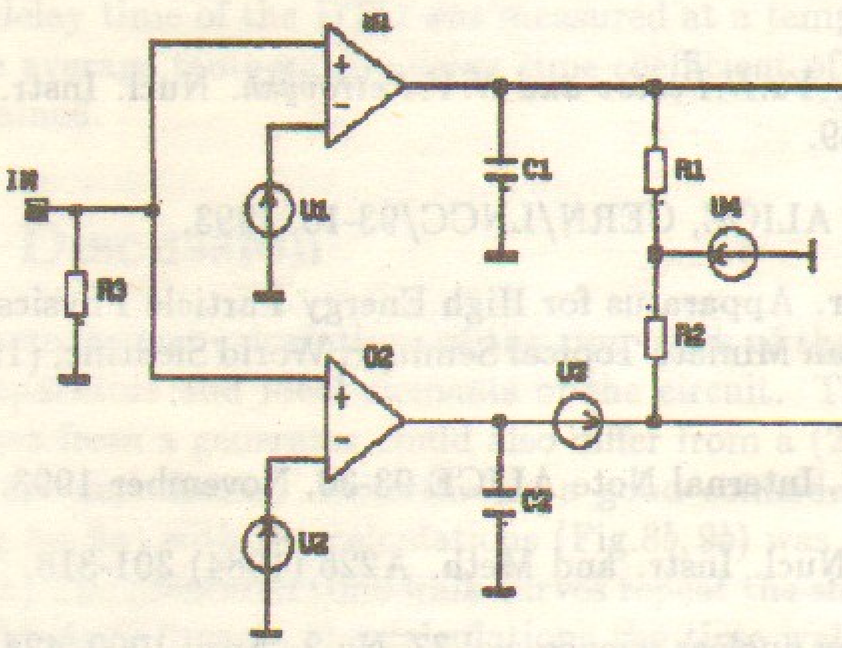

Figure 1. The double threshold discriminator block diagram.

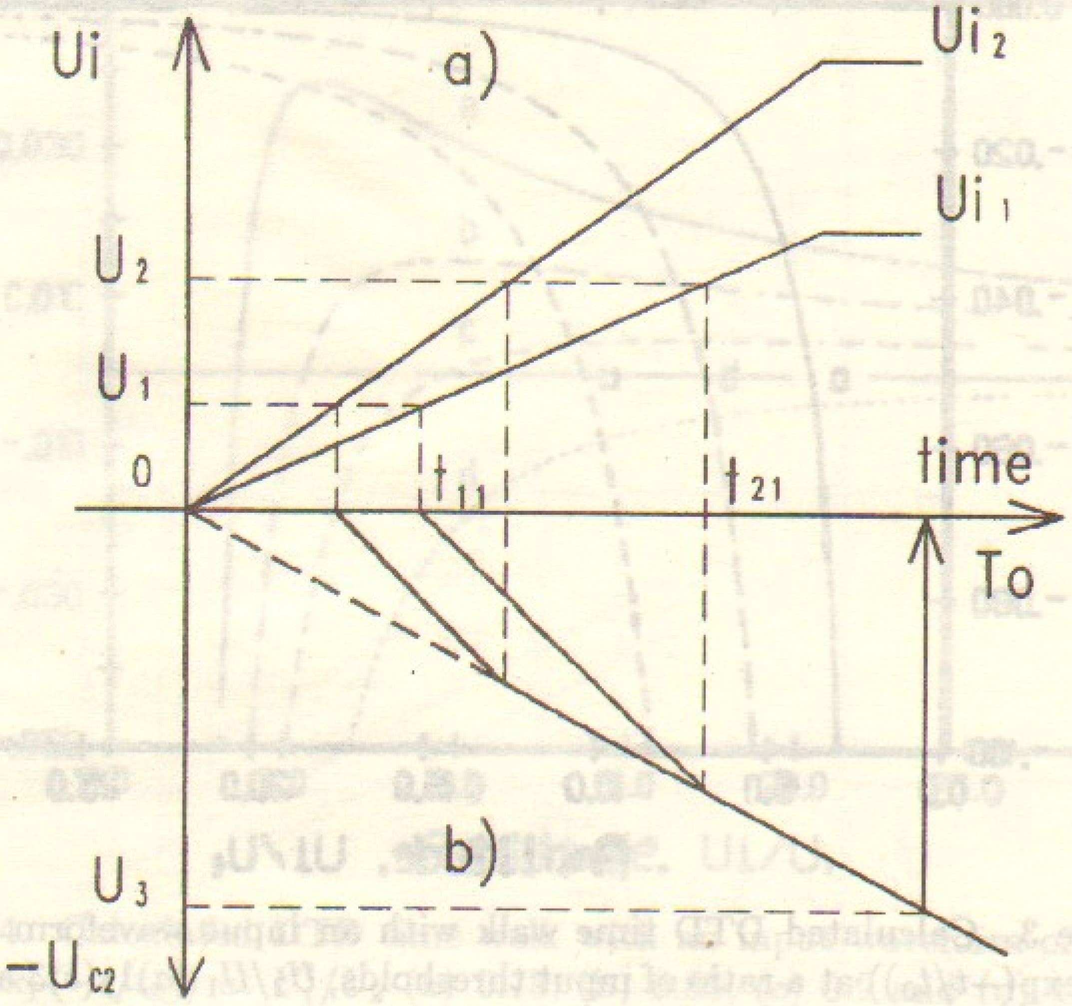

Figure 2. Illustration of a time walk compensation principle in the DTD for an input ramp. a) Time diagram of input pulses for two input amplitudes, U_{i1} and U_{i2}.b) Dependence of a potential difference at capacities C1 and C2 on time.

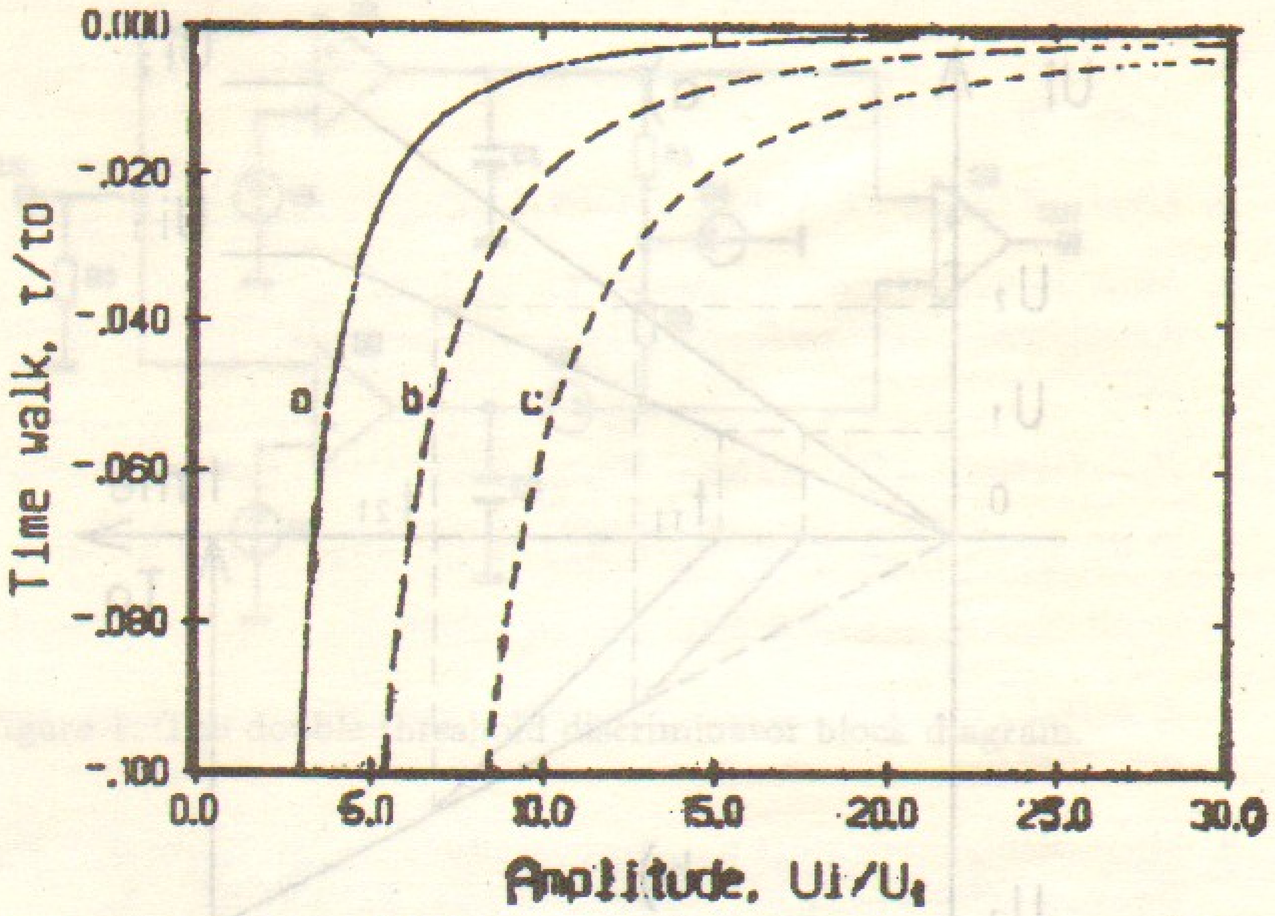

Figure 3. Calculated DTD time walk with an input waveform of $U_i = U_{i0} \cdot (1 - \exp(-t/t_0))$ at a ratio of input thresholds, U_2/U_1 $(a)1, (b)3$ and $(c)6$. The circuit parameters are optimized for a ramp.

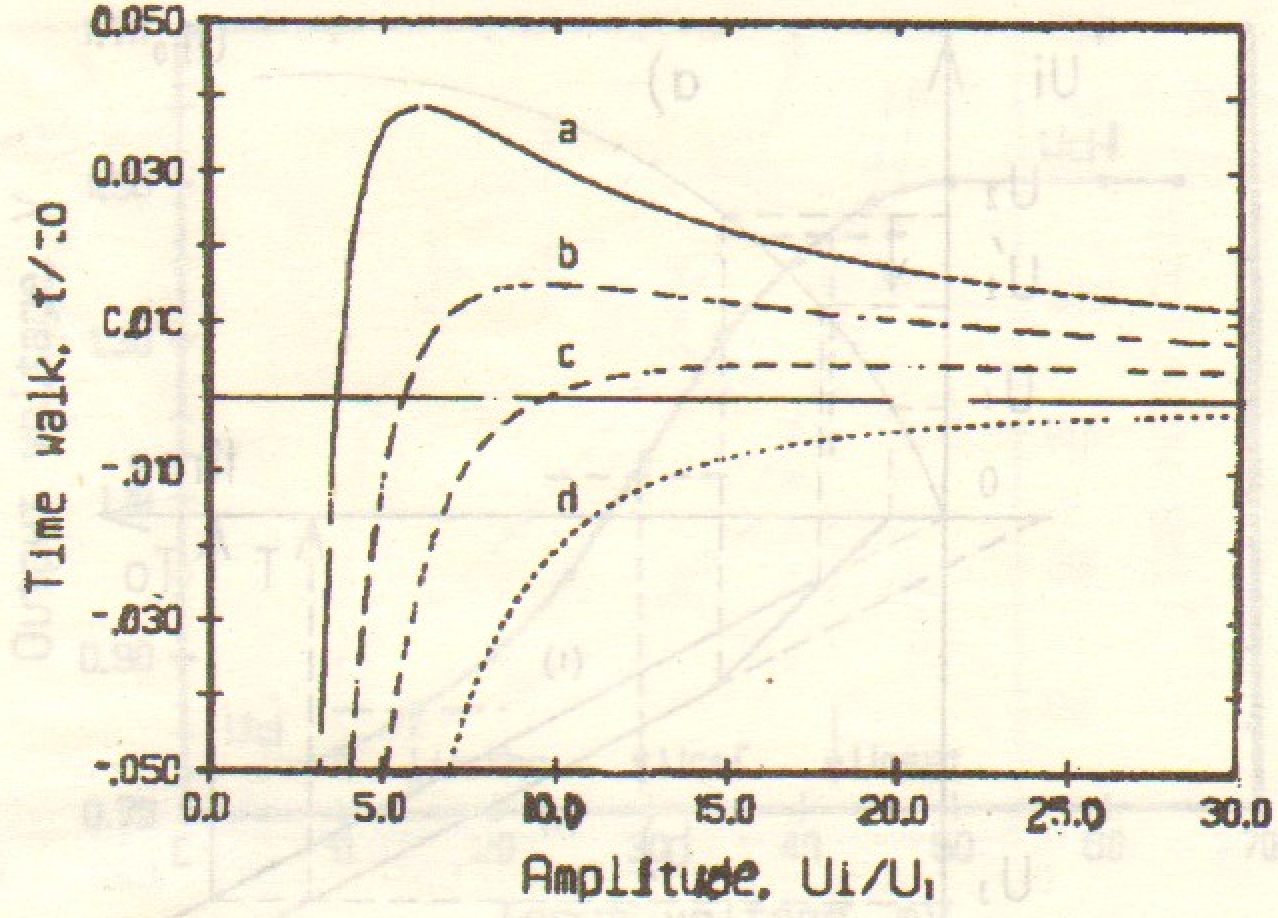

Figure 4. Calculated DTD time walk with an input waveform of $U_i = U_{i0} \cdot (1 - \exp(-t/t_0))$ at U_1'/U_2 (a) 0.75, (b) 0.83, (c) 0.9 and (d) 1. The U_2 threshold and other circuit parameter values are optimized for a ramp at $U_2/U_1 = 3$.

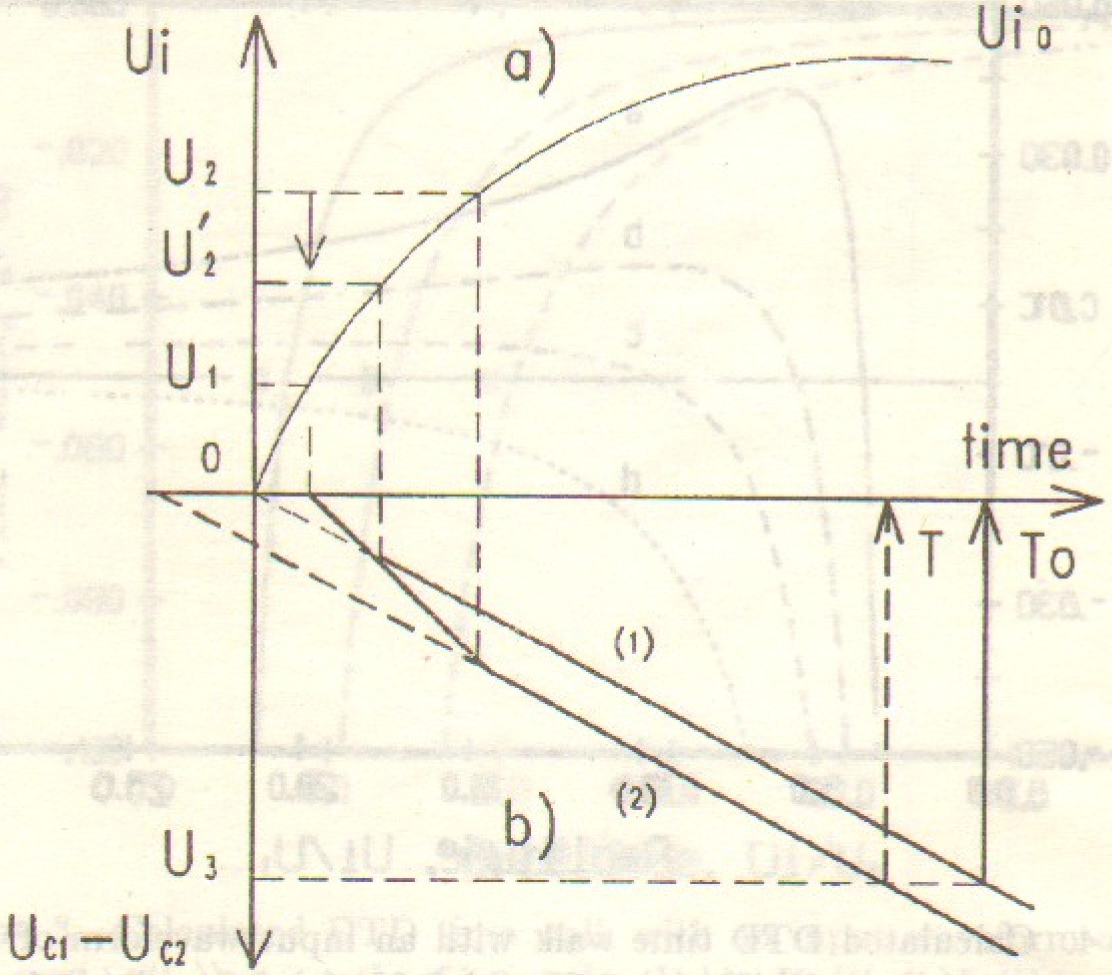

Figure 5. Illustration of choice of the U_2' threshold value corresponding to a time walk curve with crossing of the amplitude axis at U_{i0} value. An input waveform is $U_i = U_{i0} \cdot (1 - \exp(-t/t_0))$.

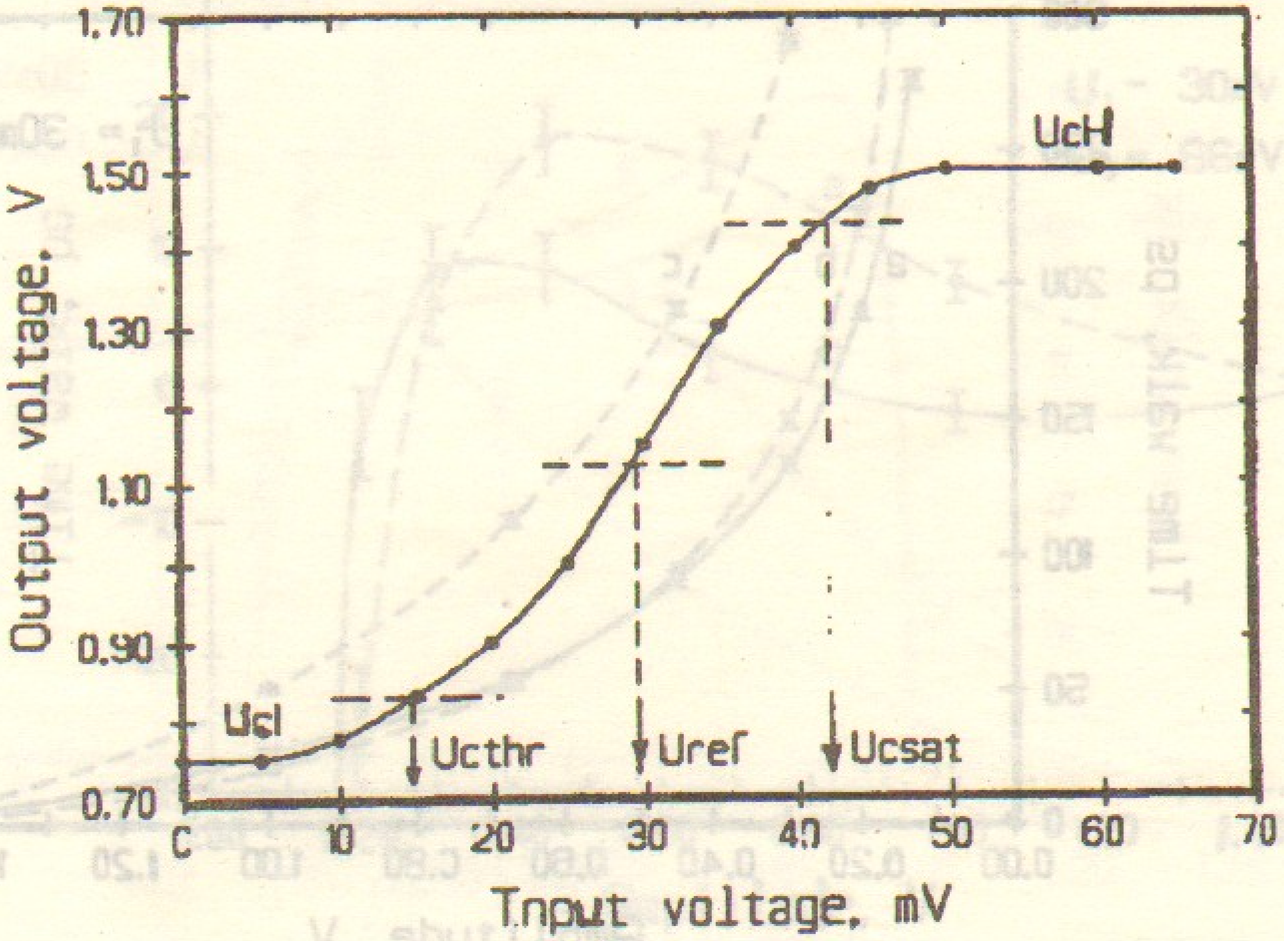

Figure 6. Input-to-output static characteristic of the K1500LP114 comparator.

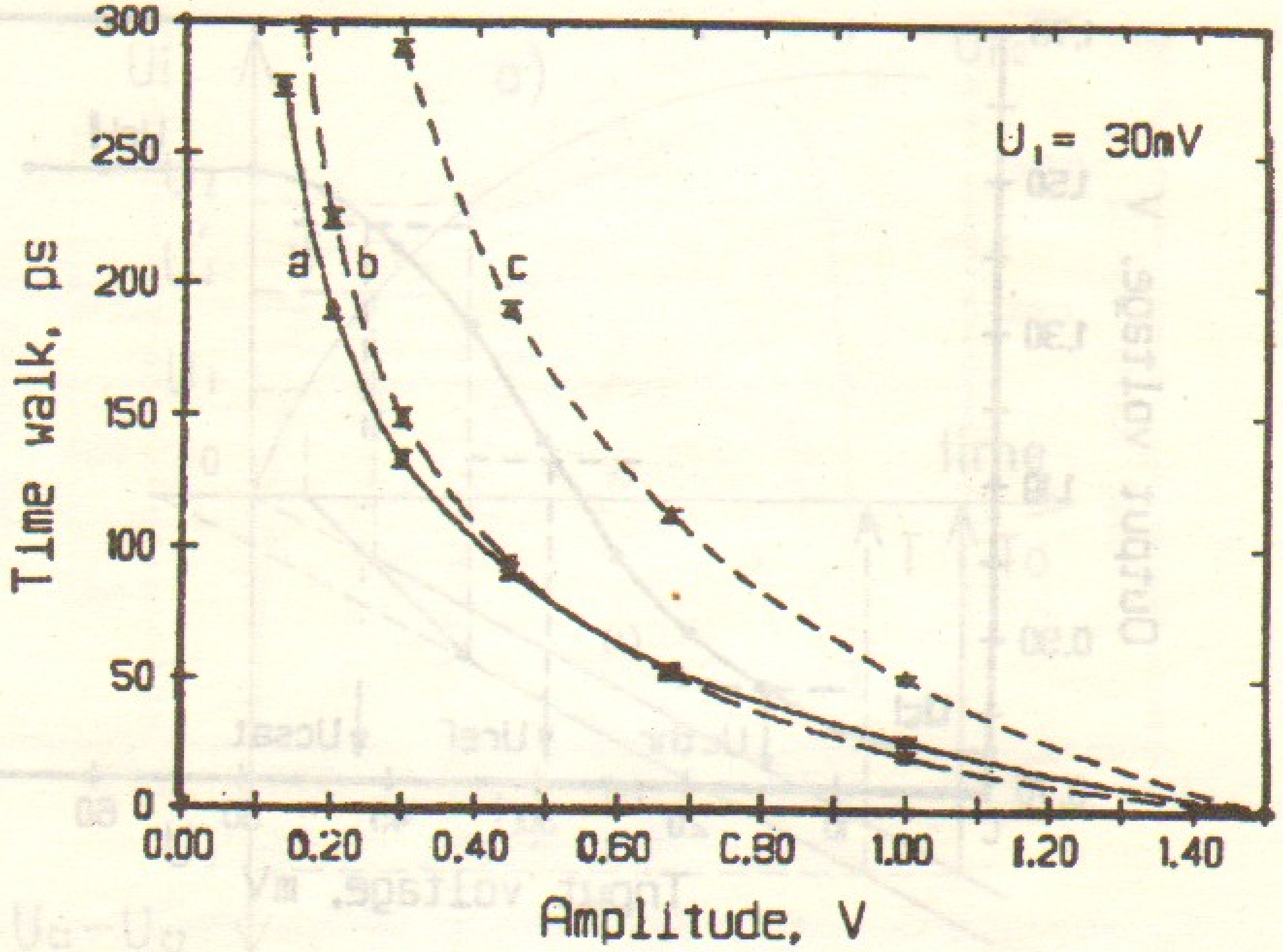

Figure 7. Time walk of the K1500LP114 comparator at an input threshold of 30 mV measured with a pulse rise time of (a) 0.2, (b) 0.8 and (c) 1.3 ns.

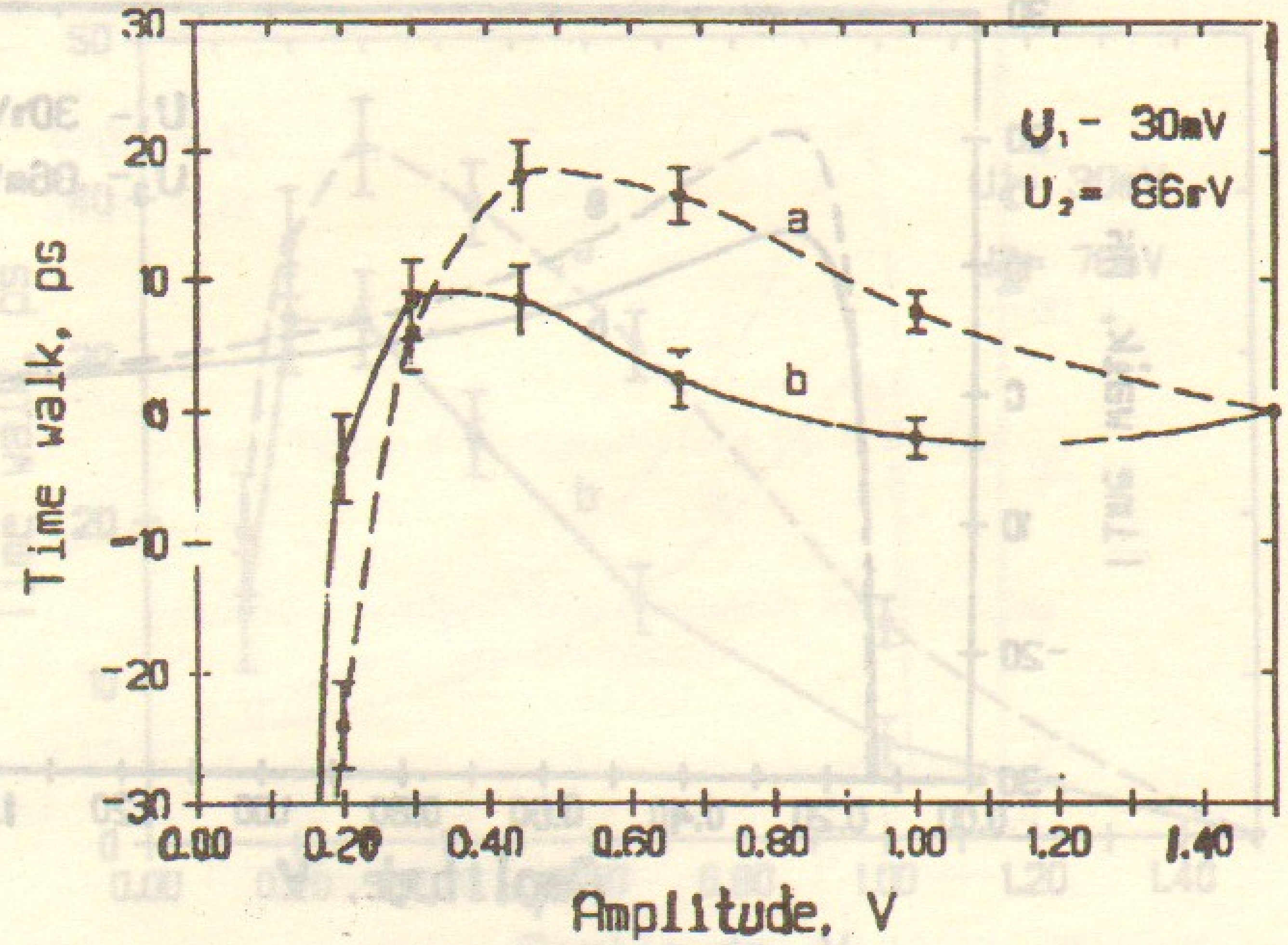

Figure 8a. Measured time walk of the DTD at the thresholds of U_1 =30 mV and U_2 =86 mV with a pulse rise time of (a) 1.3 and (b) 0.8 ns.

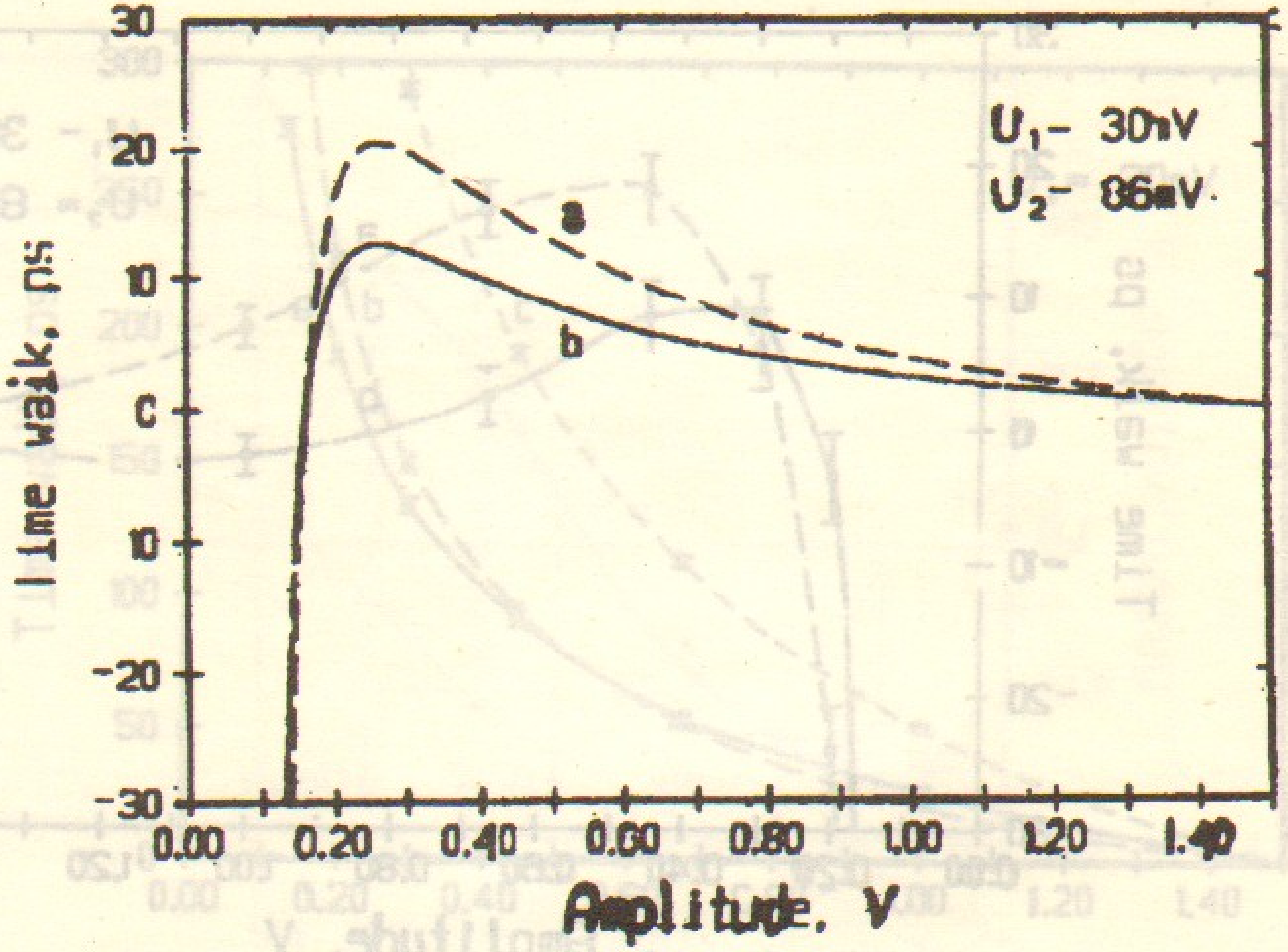

Figure 8b. Calculated time walk of the DTD at an input waveform of $U_i = U_{i0} \cdot (1 - \exp(-t/t_0))$. For other conditions see Fig.8a.

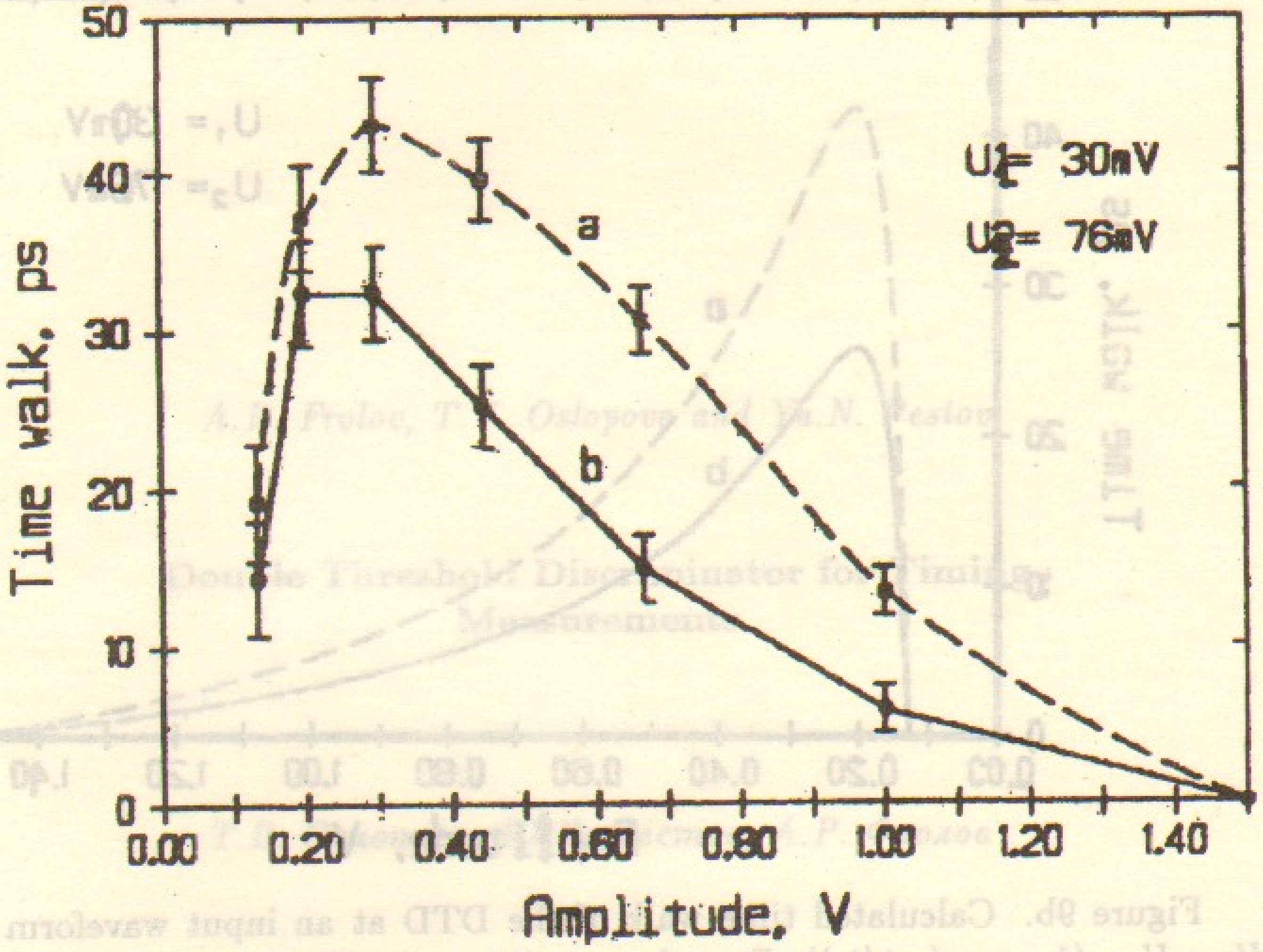

Figure 9a. Measured time walk of the DTD at the thresholds of U_1 =30 mV and U_2 =76 mV with a pulse rise time of (a) 1.3 and (b) 0.8 ns.

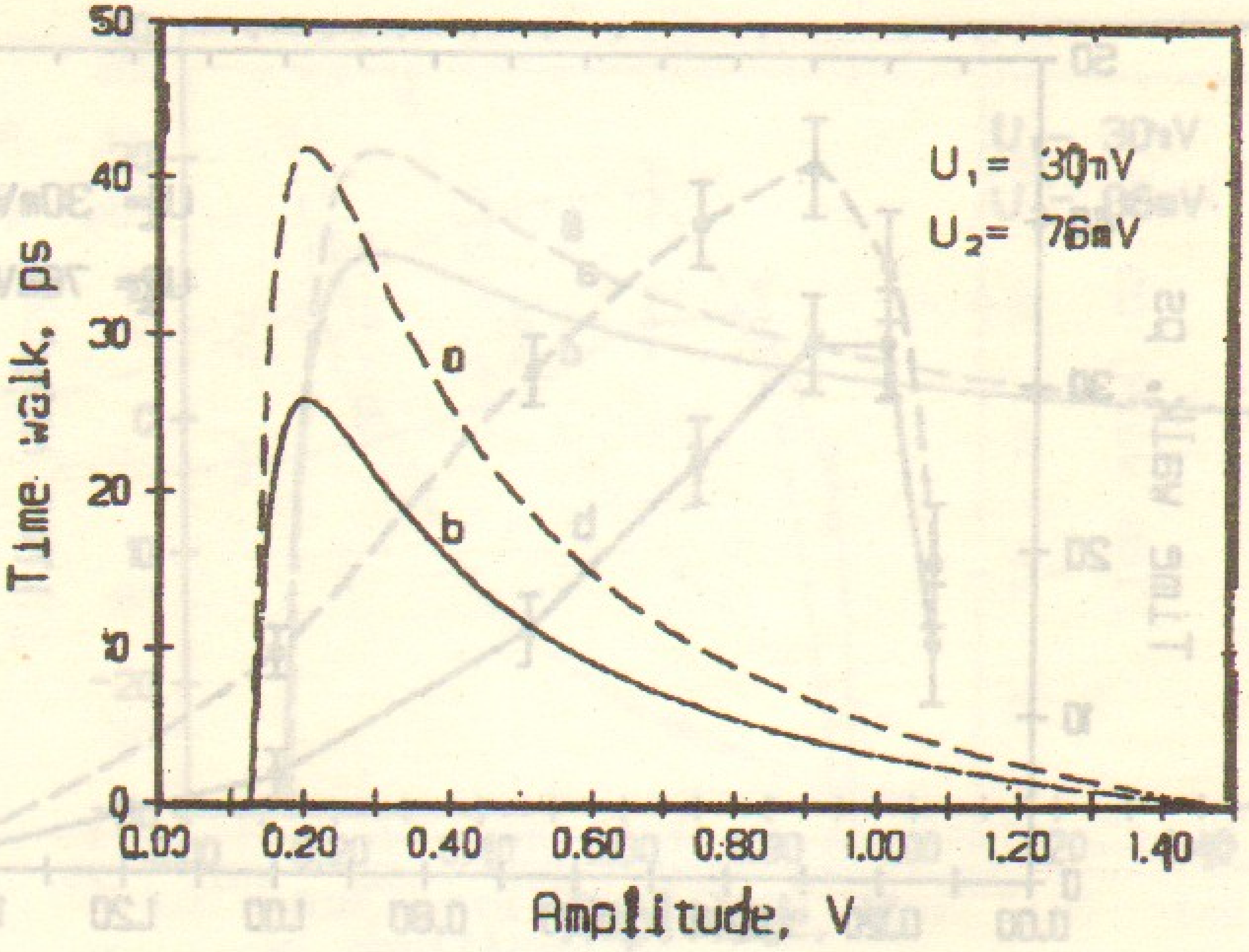

Figure 9b. Calculated time walk of the DTD at an input waveform of $U_i = U_{i0} \cdot (1 - \exp(-t/t_0))$. For other conditons see Fig.9a.

A.R. Frolov, T.V. Oslopova and Yu.N. Pestov

Double Threshold Discriminator for Timing Measurements

Т.В. Ослопова, Ю.Н. Пестов, А.Р. Фролов

Двухпороговый дискриминатор для временных измерений

Ответственный за выпуск С.Г. Попов
Работа поступила 14 апреля 1994 г.

Сдано в набор 15 мая 1994 г.
Подписано в печать 15 июня 1994 г.
Формат бумаги 60×90 1/16 Объем 1.2 печ.л., 0.9 уч.-изд.л.
Тираж 200 экз. Бесплатно. Заказ N° 31

Обработано на IBM PC и отпечатано на
ротапринте ИЯФ им. Г.И. Будкера СО РАН,
Новосибирск, 630090, пр. академика Лаврентьева, 11.